Deeply inside tunable CROW delay lines

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A chip-scale continuously tunable delay-line is presented and both experimental and numerical results are discussed. The focus of the work is mainly on the open issues, involving both theoretical and practical aspects to take care of or still to solve.

Summary

A slow-wave coupled-resonator optical waveguide (CROW) has been successfully employed to realize a tunable delay line able to introduce a continuously controllable delay of several bits on optical signals modulated at several Gbit/s [1]. Experimental results obtained with thermally activated rings fabricated in 4.5% index contrast silicon oxynitride (SiON) technology demonstrated a continuously tuneable fractional delay from 0 to 8 bits at 10 Gbit/s (overall delay 800 ps) and 25 Gbit/s (320 ps). Thanks to the high storage efficiency, exceeding 1 bit/RR, the device reconfiguration can be easily handled and the device footprint is below 7 mm^2. System performance and signal degradation were also investigated, showing a fractional loss below 1 dB/bit and error-free operation (BER < 10^{-9}) at 10 Gbit/s for fractional delays up to 3 bits.

This device is an excellent demonstration of the optimal trade-off achieved between all the variables and parameters of the structure and the synergy between the optical circuit, the technology constraint and the management of the reconfigurability. There are several critical points to tackle with and to optimize: the choice of the technology and the architecture, the impedance matching (or apodization) impacts on backreflections, the slow down factor should be high enough to increase the storage efficiency but not too high to reduce the technological sensitivity to tolerances, the limitations imposed by the index contrast, mainly the minimum bending radius, the effect of waveguide roughness, the impact of coupling coefficient disorder and phase disorder, the tuning mechanism and its management, thermal cross-talk and so on. Moreover, one has to face with waveguide losses, chromatic dispersion and impedance matching, the three main limiting factor of the ultimate performances of this architecture, and find the right trade-off to achieve acceptable system performance.

In the talk we will highlight the main features and limits, the open issues and the tricks for proper operation with a brief overview on the possible applications.

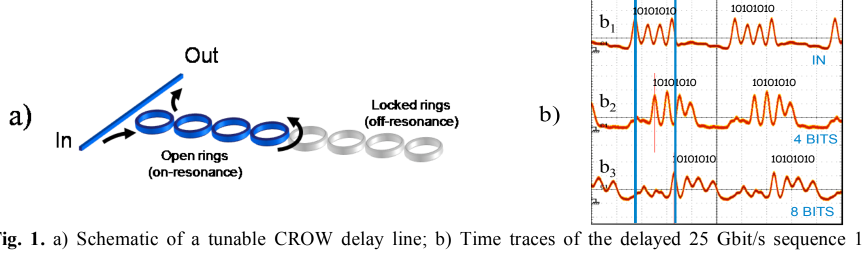

Fig. 1. a) Schematic of a tunable CROW delay line; b) Time traces of the delayed 25 Gbit/s sequence 10101010-00000000 at the output of the CROW delay line: (b_1) zero delay, (b_2) 4-bit 160 ps delay and (b_3) 8-bit 320 ps delay.

References

[1] F. Morichetti et al., "*A reconfigurable architecture for continuously variable optical slow-wave delay lines*," Opt. Express **15**, 17273, Dec. 2007.