Integrated Quantum Dot 2x2 Switch for Uncooled Switching Applications

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Abstract. *This paper demonstrates the uncooled operation of an integrated 2x2 quantum dot switch and investigates the feasibility of an uncooled 32x32 optical switch constructed using QD monolithic crosspoint switches.*

Introduction

The increasing commercial demand for next generation services such as video on demand, voice over IP, and IP television has placed a requirement for highly reconfigurable optical cross-connects (OXC) for implementation as both core and edge switches in the next generation optical networks [1]. Optical switching technologies such as optical MEMS have been of interest, but they have slow switching speeds and are relatively lossy [2]. High speed switching is considered advantageous as it would improve network efficiency and provide greater flexibility, while lossless switching would negate the need of additional amplifiers in the link. As a result, there has been increasing interest in quantum dot (QD) semiconductor optical amplifiers (SOAs) for high speed optical switching applications as they demonstrate broad gain bandwidth, low noise performance, ultra-fast gain recovery, high saturation output power and low crosstalk performance [3]. A further issue arises from the need for high port count switch fabrics to operate uncooled over a large temperature range to reduce package complexity and cost by the removal of the thermoelectric cooler (TEC) used for temperature stability. QD-SOAs have been believed for some time to have the potential for enhanced temperature performance compared with multi-quantum well (MQW) SOAs owing to their improved carrier confinement.

In this paper, we present the performance of uncooled integrated 2x2 QD-SOA switches and consider their potential for scalability to switch sizes of up to 32x32. The basis of the analysis draws from the presented measurements of high gain, low penalty switching operation in an integrated 2x2 QD SOA switch at temperatures up to 70°C [4].

Monolithic 2x2 QD Switch

The layout of the 2x2 QD SOA switch is shown in Figure 1. The switch incorporates a QD active structure which is grown on a GaAs(100) substrate using molecular beam epitaxy. The active layer comprises a ten-fold stack of $In_{0.15}Ga_{0.85}As$ QDs, separated by 33nm GaAs buffer layers, embedded in an $Al_{0.35}Ga_{0.65}As$ waveguide. Standard photolithography and ICP dry etch processes are used to fabricate the ridge waveguide structures. Each of the four input ridge waveguides has a width of 3µm which expands linearly to a 6µm width, over a length of 150 µm. At this point, a focused ion beam etched 45° TIR mirror (inset Figure 1) is used to realise an integrated beamsplitter element, which allows 50% of the signal to pass to each of the following straight and perpendicular SOA gates. For 'through' path switching, bias current is applied to the

QD SOAs in sections 1, 2, and 3. Alternatively, bias current is applied to sections 1, 4, and 6 for the 'drop' path. The switch has an overall chip area of only 2.55x0.85 mm^2.
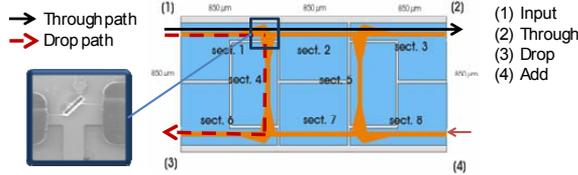

Figure 1: Schematic of switch structure showing the inputs, outputs, waveguides, splitters and SOA sections. Labels (1) to (4) denote the inputs and outputs of the switch. The solid and dotted arrows show the 'through' and 'drop' paths respectively. The TIR mirror used to route the light to drop and through path is shown in the inset.

The switch architecture considered in this analysis is based on a recently published Benes-Tree hybrid architecture [5]. This switch is similar to the Benes architecture, but with its middle cores replaced by a tree broadcast & select (B&S) architecture of corresponding size. A NxN switch designed using this architecture is shown in Figure 2A (with N as the number of inputs and outputs). It consists of N/2 2x2s in the input stage, two N/2xN/2s in the middle stage and N/2 2x2s in the output stage. Figure 2B shows how a 2x2 switching element can be augmented to a 4x4, 8x8 and 16x16 middle switching stage. Therefore, it can be seen for example that the 32x32 switch can be built using 160 2x2 switches, with each routing path traversing three cascades of 2x2 QD-SOA switches. As shown in Figure 2B, each step of switch augmentation requires an addition of one splitter at the inputs and one combiner at the output. The total number of splitters at the input and combiners at the output, as well is the corresponding net loss assuming 3.5dB passive loss for each splitter and combiner, is summarized in Table 1.
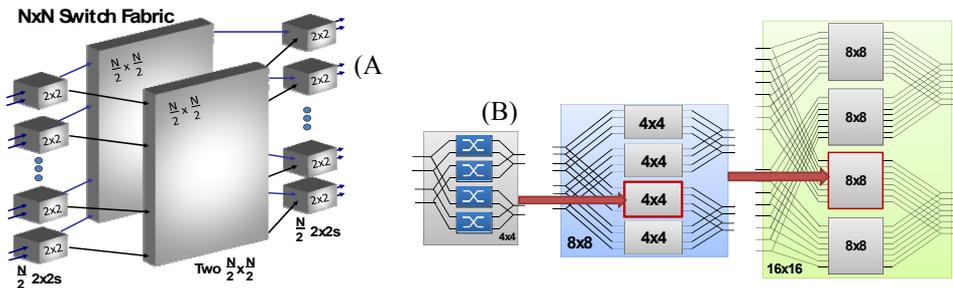

Figure 2: (A) A rearrangeably non-blocking 32x32 switch using the Benes-Tree hybrid architecture [2]. The 32x32 switches can be built using 192 2x2 switches. Each routing path would transverse three cascades of 2x2 switches. (B) Shows how a 2x2 switching element can be create successively larger 4x4, 8x8 and 16x16 switch fabric. Each step of switch augmentation requires an addition of one splitter at the inputs and one combiner at the output.

Table 1: Summary of number of input splitters and output combiner for a given switch size using 2x2 switching element and building blocks.

Switch Size for N/2 x N/2 middle stage	Number of Input Splitter	Number of Output Splitter	Total Input Splitting loss	Total Output Combiner loss
4x4	1	1	3.5dB	3.5dB
8x8	2	2	7.0dB	7.0dB
16x16	3	3	10.5dB	10.5dB

Uncooled Operation of 2x2 QD SOA Switch

Figure 3 shows the performance of the switch operating under temperature conditions between 20°C to 70°C. In figure 3A we show the gain vs. wavelength for a range of temperatures for the through path of the switch. The gain of the drop path is 3dB less owing to the excess loss of the additional mirrors to route the signal to the drop path. In general, the peak gain is higher when temperature is low, and the peak gain wavelength increases with temperature, as expected. For a 5nm optical bandwidth (1285-1290nm), there is only a ±3dB gain variation in the temperature range from 20°C to 70°C, which is shown in figure 3B.
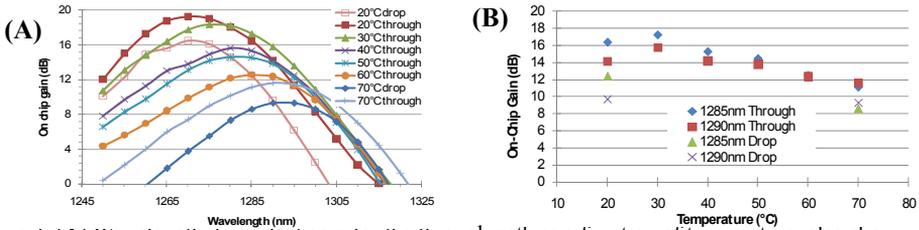

Figure 3: (A) Wavelength dependent gain for the through path as a function of temperature; also shown is the drop path at 20°C and 70°C. (B) highlights a region where gain is above 8.5dB for all temperature and ports .
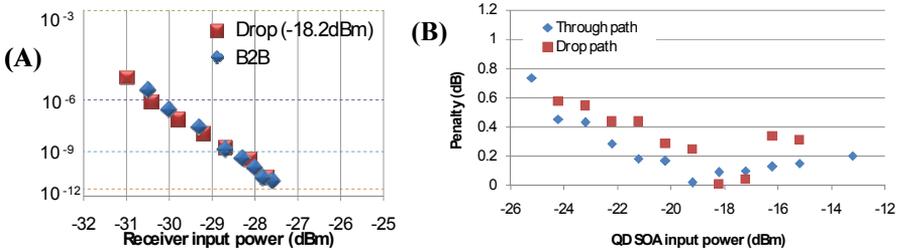

Figure 4: (A) BER curve for input power -18.2dBm. (B) Penalty vs. input power for the 2x2 QD-SOA switch at 70°C at 1290nm.

An optical signal at 1290nm wavelength, modulated with 10Gb/s PRBS sequence of 2^{31}-1, is transmitted to the 'input' power of the switch to assess the bit error rate (BER) performance from the 'through' and 'drop' output ports. The BER curve for input power -18.2dB is shown in Figure 4A, showing error free operation. The power penalty vs. input power curve for both the through and drop ports of the switch at operation of 70°C is shown in Figure 4B. A dynamic range of 11dB, restricted by measurement limitation, is obtained at power penalties of <0.6dB. No output power saturation is observed within the IPDR measurement range. A switching time of 1ns at 70°C has been measured [4], limited by the parasitics of the switch driver circuit.

Power Budget Analysis and Discussion

From Figure 3(A), it can be seen that for wavelength region of 1285 to 1290nm, a gain higher than 8.5dB can be obtained for both through and drop for all temperatures between 20°C and 70°C. It can be seen that for power penalties of <0.6dB, the input power dynamic range into the switch ranges from -13dBm to -24dBm. Hence, the power budget analysis would be based on each 2x2 switch giving a worst case gain of 8.5dB, with the maximum incurred power penalty for each stage of 0.6dB. Together

with the inter-stage switch loss information in Table 1, the evolution of power budget with the specified constraints is plotted in Figure 5.

It can be seen from Figure 5 that the estimated input power dynamic range of 11dB, 11dB and 7dB are obtained for switch sizes 8x8, 16x16 and 32x32 respectively. However, as calculations are based on IPDR measurements carried out using experimentally measured parameters for 1290nm wavelength, 70°C temperature and 100mA bias current, several assumptions have to be made. Overshoot of the 'IPDR max' region is considered acceptable as the gain of the QD-SOA can be reduced to operate within the IPDR margin by using a lower bias current. The reduction of gain is assumed not to incur additional penalties over the region of interest as lower bias current would contribute less amplified spontaneous emission (ASE) noise to the signal. As for the changes in temperature, similar IPDR measurements of a QD 2x2 SOA have been previously carried out at 20°C and penalties of <0.2dB have been measured over the region of interest [6].
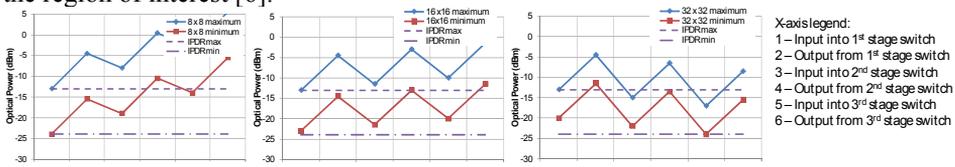

Figure 5: Figure shows the power budget evolution for switch sizes of 8x8, 16x16 and 32x32. The numbers (1 to 6) x-axis of the graph corresponds to the point of the signal within the switch, as shown in the top sub-figure.

Conclusion

This paper investigates the potential to realise high speed optical switches of size up to 32x32, operating uncooled over a temperature range of 20 to 70°C, using cascades of integrated 2x2 QD SOA switches. This analysis is derived from uncooled static and dynamic measurements of a fully integrated QD-SOA switch, which in the wavelength region of 1285 to 1290nm has a maximum of 17dB and minimum of 8.5dB gain, and an IPDR of 11dB (restricted by measurement limitations) at temperatures up to 70°C for power penalties of <0.6dB. The estimated input power dynamic range of the switches are 11dB for 8x8, 10dB for 16x16 and 4dB for 32x32 for cumulative power penalties of 1.8dB and below. These results show the significant potential of QD SOA technology in uncooled optical switched networks.

References

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