

Optical Buffer Memory Using Polarization Bistable Vertical-Cavity Surface-Emitting Lasers

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Abstract: A novel optical buffer memory with shift register function is proposed. The buffer consists of a two-dimensional array of polarization-bistable vertical-cavity surface-emitting lasers (VCSELs), in which the bit state of the optical signal, “0” or “1” is stored as a lasing linear polarization state of 0 or 90°. Two-bit optical buffering is experimentally demonstrated using two 980 nm polarization-bistable VCSELs having a mesa structure.

Introduction

Optical packet switching is emerging as a potentially important technology in optical networks. To handle the contention of output ports at an optical packet-switching node, a high-speed, low-power optical memory for buffering data is required. A fiber-loop-type buffer equipped with a gate has been proposed¹. However, these all-optical buffers are unable to access the data randomly at an arbitrary timing. Optical flip-flop memories, in which one bistable device acts as a one-bit memory, are also potentially applicable to this scenario². Two configurations for achieving fast and low-power bistable optical devices have been reported: a polarization-bistable vertical-cavity surface-emitting laser (VCSEL)³, and a coupled micro-ring laser⁴. Optical shift registers have received considerable attention and several approaches have been explored, including an optical shift register based on cascaded optical flip-flop memories driven by common optical clock pulses⁵. This concept has also been realized using coupled self electrooptic effect devices (SEEDs) driven by changes of the driving voltage⁶.

The existence of pitchfork bifurcation bistability through gain saturation in laser diodes has been predicted theoretically⁷, and has been observed experimentally as polarization bistability in VCSELs⁸. The polarization bistable operation in a VCSEL is shown schematically in Fig. 1. The VCSEL with square mesa structure exhibited bistable polarization switching between 0° polarization and 90° polarization⁸. The VCSEL initially oscillated with 90° linear polarization, but switched permanently to 0° linear polarization upon injection of a 0° polarized optical trigger pulse. The polarization switch was reversible upon injection of a suitable 90° polarization trigger pulse. The polarization state did not change upon injection of an optical trigger input with the same polarization as the current VCSEL state. This polarization-bistable

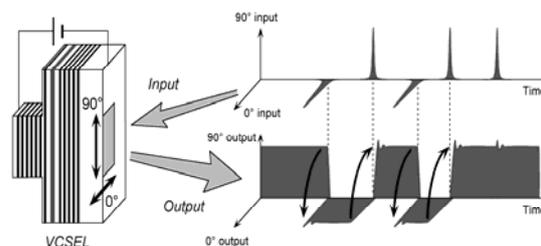


Fig. 1: Bistable polarization operation in a VCSEL

VCSEL is thus usable as an AND or OR gate. In previous experiments using VCSELs⁹, ultrafast polarization switching with 7 ps switching-time was successfully demonstrated in all-optical flip-flop operation³. Switching energy of just 0.2 and 0.3 fJ has also been achieved for the set and reset optical pulses, and a switching frequency of 10 GHz has been demonstrated in flip-flop operation¹⁰.

In this presentation, a novel optical buffer memory with shift register function is discussed. The buffer is based on a two-dimensional (2D) array of polarization-bistable VCSELs, and is experimentally demonstrated to realize optical buffering, involving the sequence of selective storage of signal bits from a four-signal-bit train, readout of the stored signals with an appropriate time delay, and finally erasure of the stored signals.

Principle of optical buffer memory

Using a 2D array of polarization-bistable VCSELs, a novel optical buffer memory can be constructed, as shown in Fig. 2^{11,12}. The polarizations of the VCSELs in the first column (M_{1x}) are reset to 0° by injection of an optical reset pulse with 0° polarization. The ultrafast optical signal is converted to spatially parallel signals by a time-to-space converter, and the parallel set of signals is injected into the VCSELs together with optical set pulses. The power of the optical signals “1” and the optical set pulse are weaker than the polarization switching threshold, but the sum of the powers of the two inputs exceeds the threshold. Thus, the VCSELs only change polarization (from 0 to 90°) when the optical signals “1” and the optical set pulses are injected simultaneously into the VCSELs (i.e., AND gate operation). The output of each VCSEL of the first column is thus polarized depending on the bit state (“0” or “1”) of the input signal which is injected with the set pulse simultaneously. The optical gates

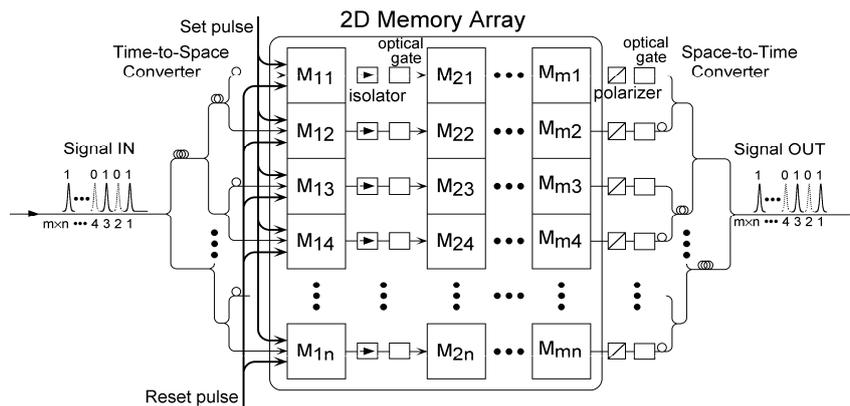


Fig. 2: Proposed optical buffer memory with shift register function

between the first column (M_{1x}) and the second column (M_{2x}) are then opened, and the optical outputs of M_{1x} are injected into M_{2x} via optical isolators. The data stored in M_{1x} are transferred to M_{2x} and held as memory, since the polarizations of the M_{2x} array switch to match those of M_{1x} . Only the 90° outputs from the VCSELs of the last column (M_{mx}) transmit through polarizers. The output signal pulses are created from the CW outputs of the VCSELs using optical gates, and are converted to an ultrafast optical signal by a space-to-time converter. This circuit thus provides an optical buffer memory with shift register function. This shift register function allows continuous and long data to be stored, and simplifies the design of the time-to-space and space-to-time converter, both of which can now be constructed using optical fibers of appropriate lengths and 3 dB couplers. This makes it possible for the converters to be integrated into silicon-based planar lightwave circuit (PLCs) or semiconductor integrated waveguides. As optical gates that are inserted between columns and at the output of the VCSEL, LiNbO_3 modulators were used in the present experiments. However, ultrafast all-optical switches should be used for higher signal bit rates. These features provide advantages such as the potential for large-scale 2D VCSEL arrays.

Polarization bistable VCSEL

A 980 nm VCSEL was used as the memory element (Fig. 3). This VCSEL has InGaAs active layers and AlGaAs distributed Bragg reflectors (DBRs)¹³⁾. The p-type DBR was processed to a $5 \times 4.5 \mu\text{m}^2$ rectangular post-structure and was buried with a polyimide layer. The VCSEL lased in the lowest-order transverse mode. The lasing polarization was one of the two linear polarizations of 0 and 90° , and polarization switching was observed at approximately 6.7 mA with hysteresis of about 0.6 mA in operation at 15°C . The typical side-mode suppression ratio (SMSR) determined from the measured polarization resolved spectra was 34 dB, indicating stable laser oscillation in the lowest-order transverse mode. The typical value of the orthogonal

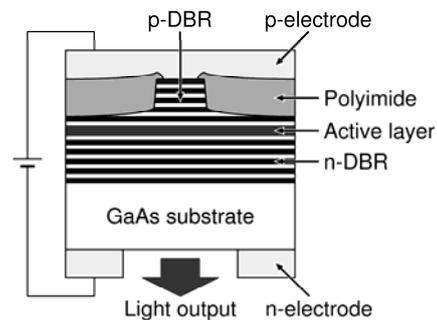


Fig. 3: Schematic structure of VCSEL as a memory element

polarization suppression ratio (OPSR) was 23 dB. All-optical flip-flop operation was obtained with injection of a $9.6 \mu\text{W}$ set pulse and $9.2 \mu\text{W}$ reset pulse.

One-bit optical buffering

The circuit described above was successfully used to perform one-bit optical buffering in experiments. A timing chart for the optical buffering is shown in Fig. 4 for both “1” and “0” signals. The injection power of the data signal and set pulse is set less than the polarization switching threshold in order to obtain AND gate functionality. In the case of “1” signals, when both the data signal and set pulse are injected simultaneously, the injection power exceeds the polarization switching threshold and the lasing polarization of the VCSEL is switched from 0 to 90° . Thus, b_1 of the data signal is stored as the polarization state of the VCSEL. The 90° polarization component of the VCSEL output is read as the readout signal by opening an optical gate. A reset pulse is finally injected, and the lasing polarization of the VCSEL returns to 0° . In the case of “0”, the sum of b_1 and the set pulse power does not exceed the threshold, causing the lasing polarization of the VCSEL to remain at 0° . A “0” signal is then readout by applying a gate pulse.

Figure 5 shows the setup. The injection lights for the data signal, set pulse and reset pulse were generated by tunable external cavity laser diodes (EC-LDs) and LiNbO_3 modulators, and were polarized to 90 or 0° by polarization controllers (PCs). The VCSEL was

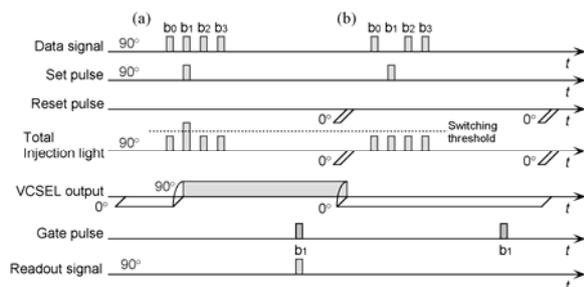


Fig. 4: Timing chart for one-bit optical buffering

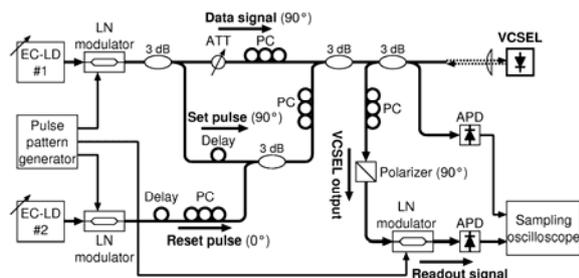


Fig. 5: Experimental setup for demonstration of one-bit optical buffering

operated at an injection current of 5.8 mA, output power of 28 μ W, and temperature of 20 $^{\circ}$ C. A readout signal was created from the 90 $^{\circ}$ component of the CW output of the VCSEL by a LiNbO₃ modulator.

The experimental results are shown in Fig. 6. Due to limitations with respect to pattern generation, the injection lights include unnecessary pulses, but these do not affect the operation of the optical buffer memory. The data patterns were set to “1111” in the first half and “1011” in the later half of the run. The timing of the set pulse was adjusted to that of the 2nd bit of the data signal. The lasing polarization of the VCSEL was switched from 0 to 90 $^{\circ}$ only in the first half, remaining at 0 $^{\circ}$ in the later half. Readout signals corresponding to the 2nd bits of the data signal were obtained, demonstrating one-bit optical buffering.

Two-bit optical buffering

Principle of the two-bit optical buffer memory is shown in Fig. 7. A data signal and a set pulse are a linear polarization of 90 $^{\circ}$. The data signal is divided into two (data signal (bit 1) and data signal (bit 2)) and data signal (bit 1) is delayed for one-bit period. The data signal (bit 1) and the data signal (bit 2) are injected into VCSEL 1 and VCSEL 2, respectively, together with the set pulse. Each injection power of the data signal and the set pulse are set to be less than the polarization switching threshold of the VCSEL. When both of the data signal and the set pulse are injected simultaneously, the injection power exceeds the polarization switching threshold and the lasing polarization of the VCSEL is switched from 0 $^{\circ}$ to 90 $^{\circ}$. Therefore, b1 and b2 of the data signal are stored as the polarization states of VCSEL 1 and VCSEL 2,

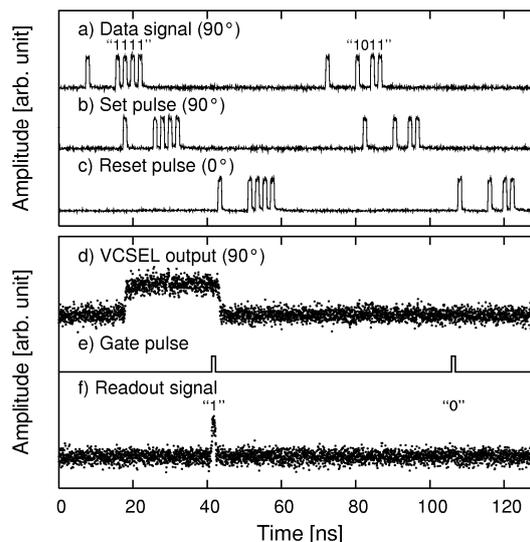


Fig. 6: Experimental results of one-bit optical buffering

respectively. Then, 90 $^{\circ}$ polarization component of the VCSEL outputs are gated and are multiplexed for the memory output. Finally a reset pulse of 0 $^{\circ}$ polarization is injected, and the lasing polarizations of the VCSELs return to 0 $^{\circ}$.

Figure 8 shows the experimental setup of 2-bit optical buffering. The data signal was divided into two parts and one data signal was delayed for one-bit period. In order to perform the polarization switching of two VCSELs using the injection lights with the same wavelengths, the lasing wavelengths of the VCSELs were tuned by controlling the device temperature. To construct a serial data stream, one VCSEL output was combined with another VCSEL output with one bit period delay. Other parts were the same as the experiment shown in Fig. 5.

Experimental results are shown in Fig. 9¹⁴⁾. The data sequences were set to four patterns of “1001,” “1011,” “1101” and “1111.” The 2nd and 3rd bits of the data sequences were stored as the polarization states of VCSEL 1 and VCSEL 2, respectively. The memory output signal had four bit patterns of “00,” “01,” “10” and “11” that correspond to 2nd and 3rd bits of the data sequences. Therefore 2-bit optical buffering has been successfully demonstrated.

Assuming the development of key technologies such as appropriate time-to-space and space-to-time converters, the number of bits that can be stored in this buffer memory is ultimately limited by the electrical power consumption of the VCSEL. If the bias current can be reduced to 1 mA, a single VCSEL consumes 1 mW at 1 V. Thus, a single 1000 \times 100 2D array of VCSELs provides 100 kbits of optical memory, but requires 100 W of power. Arrays of this size will be required for all-optical routers with small integrated optical buffers as small as 10-20 packets (80-160 kbits)¹⁵⁾. Substantial improvements in the buffer memory are considered possible. The VCSELs of the first column (M_{1x}) should operate

with high-speed. For the other VCSELs ($M_{2x} \sim M_{m-1x}$), low power consumption is the most important factor. Optical output of the VCSELs of the last column (M_{mx}) should be high. For low power consumption, photonic bandgap defect cavity lasers having an optical mode size as small as $0.5 \mu\text{m}$ in diameter¹⁶⁾ can be used.

Conclusion

A novel optical buffer memory consisting of a 2D array of polarization-bistable VCSELs and providing shift register functionality was proposed. One-bit optical buffering was experimentally demonstrated, involving selective storage of a signal bit from a four-signal-bit train, readout of the signal with an appropriate time delay, and erasure of the stored signal. 2-bit optical buffering has also been experimentally demonstrated using two polarization bistable VCSELs. These experimental results,

therefore, showed a technological feasibility of a multi-bit optical buffer memory. The authors have also demonstrated experimentally shift register function very recently. Input data stored as the polarization states of the first VCSEL were transferred to the polarization states of the second VCSEL by injection of the output from the first VCSEL to the second VCSEL.

Acknowledgments

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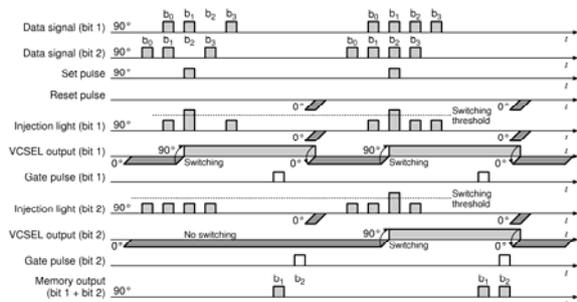


Fig. 7: Timing chart for 2-bit optical buffering

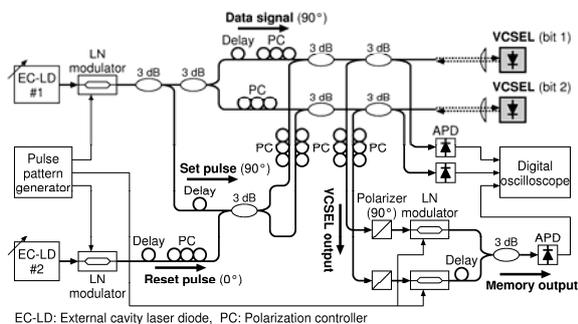


Fig. 8: Experimental setup for 2-bit optical buffering

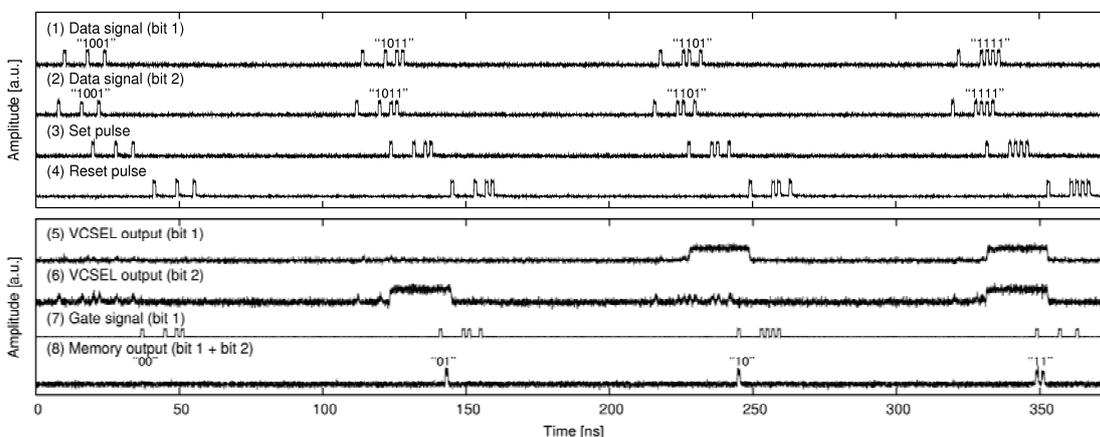


Fig. 9: Experimental results of 2-bit optical buffering