

# How complex can integrated optical circuits become?

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**Abstract:** *The integration scale in Photonic Integrated Circuits will be pushed to VLSI-level in the coming decade. This will bring major changes in both application and manufacturing. In this paper developments in Photonic Integration are reviewed and the limits for reduction of device dimensions are discussed*

## Introduction

Photonics is a rapidly growing sector in the global economy. Optical communications, optical disks, digital cameras, lighting, lasers and optical sensors are just a few examples. In comparison to electronics, most photonic equipment is still large and expensive. Just like in micro-electronics, many applications can be realized in a much more compact and cost-effective way by integrating the required functionality in a single chip.

So far, the progress in photonic integration has been hampered by the large variety in photonic devices and technologies, and the fact that most integration technologies are specific for the applications for which they have been developed. As a result the market for integrated photonics is too fragmented to justify the investments for developing an integration technology to a level that really leads to substantial cost reductions, and this, in turn, prevents rapid growth of the applications.

The way to break out of this cycle is by developing a generic integration technology with a level of functionality that can address a broad range of applications. Such a technology, which should be made accessible via foundries, can address markets that are sufficiently large to pay back the development costs. This is quite similar to what happened in microelectronics.

The power of micro-electronic integration technology is that a broad class of electronic functionalities can be synthesized from a small set of elementary components, such as transistors, resistors and capacitors. A technology that supports wafer-scale integration of these elementary components can, therefore, be used for a broad class of applications, and investments made in its development are paid back by a large market.

In a similar way, the key for the success of integration in photonics is to realize a broad range of optical functionalities with a small set of elementary components, and to develop a generic wafer-scale technology for integration of the elementary com-

ponents, thereby reducing the variety in components and technologies, and to make this technology available through a fabless approach using a foundry model, and set up libraries and a proper design and training environment to support potential users of the facilities.

In this way the development of photonic integration technology can gain sufficient momentum to achieve the substantial cost reductions that are necessary to penetrate in mass markets. The rapidly emerging market for broadband access (FTTH) is such a market. Once this happens photonic integration can enter into a similar dynamics as we are seeing now for more than three decades in micro-electronics, i.e. a steady increase in functionality at an essentially constant price, a development which can only be sustained by a steady innovation of the integration technology.

Just like in electronics, where CMOS doesn't provide the answer for all problems, a single generic technology will not be able to cover all applications, if it were only because of the quite different wavelength windows required by different applications. So we will need a few technologies to cover the whole field. But it will be a small (but powerful) subset of the multitude that we have today, and some of them may eventually merge into a technology that combines the best of photonics and electronics into a hybrid or heterogeneous integration platform.

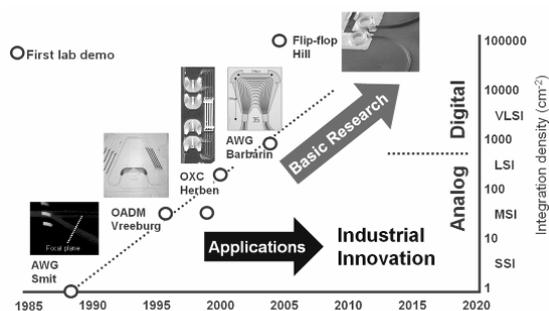
In the present paper we will focus on semiconductor-based integration technology (InP), which is a key technology for large scale photonic integration. In the last section we will pay some attention to other technologies.

## Moore's law in Photonics

The field of Information and Communication Technologies is showing a development speed which is unprecedented in history. Over a period of more than thirty years key features like processor speed and memory size are roughly doubling each 18 months. It is known as Moore's law [2] and enabled by the development of micro-electronic integration technology. There have been several attempts to map the development of Photonic Integration on a Moore-like plot, with circuit complexity or integration density mapped logarithmically against time. However, due to the large variety in components and technologies, one ends up with a

scattered cloud of data points that provides little insight.

If we restrict ourselves to devices realised in a similar technology, which is actually also the case in the famous Intel plot [2], a clear trend becomes visible as shown in **Figure 1** for InP-based WDM-PICs [3]. This plot, of which we presented the first version in 1995 (IEEE/LEOS Annual Meeting), appears to be surprisingly valid today, more than ten years later and it is very useful for explaining trends in photonics. The plot shows an increase in integration density of around two orders per decade, which is roughly the slope of Moore's law. It should be noted that the vertical axis does not refer to circuit complexity, but to the number of (basic) components that fit on 1 cm<sup>2</sup>, which is about the maximum size of a chip. So they are indicative for the maximum achievable circuit complexity, but practical circuits are usually smaller. The main drivers of the size reduction are increasing lithographical resolution and increasing refractive index contrast, as explained by Baets in [4].



**Figure 1** Moore's law in photonics for PIC's developed at COBRA.

The data points shown are first laboratory demonstrators. Early commercial realisations follow the line with a delay in the order of 5 years. The most recent example is the 10-channel WDM transmitter chip with a capacity of 100 Gb/s (10x10 Gb/s), that is applied by Infinera in its WDM systems [5]. It integrates over 40 components in a single chip: 10 tunable DFB-lasers, 10 EA-modulators, 10 VOAs, 10 monitor-diodes and a 10-channel AWG. Although Infinera does not reveal the chip size the density is probably around 500 components per cm<sup>2</sup>, which fits well into the metrics of **Figure 1**.

### Analog PICs

An interesting question is how long this increase in density and complexity will continue. Infinera announced already a chip with over 200 components per chip, by increasing the channel count of its device from 10 to 40 [5]. On a longer term even larger channel counts will appear, but it is unlikely that in this way, by increasing parallelism, the complexity will exceed a component count of 1000 per chip. The alternative is serial integration, but also along

this line it is improbable that the 1000 components/chip barrier will be broken. The main reason for this is that today's PICs, although they usually carry digital signals, operate essentially in an analog mode. As a result, errors generated by the components will cumulate and, after having passed a number of components, the signal will be degraded so strongly that it has to be regenerated. On-chip signal regeneration is possible, but full regenerators are complex and they also require a significant amount of chip space. Breaking the 1000 components/chip barrier by serial integration is, therefore, also unlikely. A combination of serial and parallel integration may bring us close, but we expect that for analog PICs the increase in complexity will saturate around or below 1000 components/chip. But this is not the end of Moore's law for Photonics.

### Towards Digital PICs

In the early days of micro-electronics analog circuits, such as operational amplifiers, formed an important market. Their complexity was typically limited to a few hundred components per circuit. Signal integrity was maintained by the application of feedback, but this limits the circuit complexity because feedback over too long distances reduces the speed and may cause instabilities. A real breakthrough towards VLSI required, therefore, digital circuits that operate essentially with only two levels, so that the signal is inherently regenerated after each operation and cascading of hundreds of signal operations becomes possible with virtually no signal degradation.

In photonics digital signal processing is still in an embryonic stage. A number of papers on flip-flops or logical gates have been published, but their size, speed and power consumption is such that they allow only for very small integration levels and they are by far not competitive with modern electronics.

Recently a breakthrough in digital photonic signal processing has been reported by Hill [6]: a photonic flip-flop based on two coupled microring lasers with dimensions of 20x40 μm<sup>2</sup>, a switching time of 15 ps and a switching energy of a few femtojoules. Although the device is still considerably larger than an electronic flip-flop, its dimensions allow for integrating hundred thousands of these components on a single chip, which is an integration complexity far beyond today's imagination. Its switching speed is comparable to that of high-speed electronic transistors, its switching energy is smaller by more than three orders. With some modifications (adding additional input waveguides) the device can also be used as a logical gate, so that the coupled microlasers form a basic building block for both digital photonic signal processing and storage.

From **Figure 1** it is seen that this device does not fit into the Moore's law metrics, it is more than a dec-

ade ahead. This is due to the fact that, although it is realised in a similar technology as the other devices in the plot, the flip-flop element is much smaller than the basic elements (AWGs, switches) used in the other devices. This underlines the potential of this kind of technology for VLSI.

An important issue for digital photonics is the competition with electronics. Analogue photonics brings a number of functionalities that are difficult to realise with electronics, especially for high speed signal processing. But as soon as we go to digital signal processing we will have to beat electronics in a field where it is extremely strong. Although the whole field is still very young a few applications where digital photonics will become competitive are already visible. An important one is header processing in all-optical packet switched networks, where huge electronic routers are required to switch the Terabit datastreams that occur in high-level networks. In such networks digital photonic header processing may lead to a substantial reduction of the amount of high speed electronics that is required in the routers. But when the performance of digital photonics increases more applications can be envisaged and also operations like high-speed Optical Time Domain Demultiplexing, which are now performed by rather sensitive analog optical circuitry, may be performed by digital photonic circuits.

#### Where are the limits?

It is clear that the device reported in [6] is only a first step into a new field of photonics, and it is an interesting question how far we can get before we encounter the fundamental limits of digital photonic signal processing.

An advantage of photonics over electronics is that it does not incur the charge displacements which form the speed bottleneck in electronic switching. Photonics can, therefore, operate at a higher speed than electronics, in principle, its switching speed is limited by the time that light needs for effective interaction in the switching structure. In nanocavities this time can be far into the subpicosecond domain. Electronics has the advantage that it can store information (charge) with virtually no power consumption. This is not possible in coupled lasers, they consume the same power in static and dynamic operation. We expect, therefore, that for ultrafast processing, including some short term memory functions, photonics may turn out to be superior to electronics, but for longer-term storage electronics will remain superior.

Whether photonics will really become an option for digital signal processing depends on how far features like component size and power consumption can be reduced. The microring lasers used in [6] had a ring diameter of 16  $\mu\text{m}$ , and a threshold current of 30 mA. Much smaller lasers have been reported, such as the Photonic-Crystal micro-cavity

lasers by Park [7], which have dimensions of a few micrometers and a threshold current of 260  $\mu\text{A}$ . Logical gates based on such a laser will combine sub-ps switching times with sub-femtoJoule switching energies. Although the required injection currents are still prohibitive for integrating millions of such lasers, results reported on other microcavity lasers suggest that threshold currents can become so small (a few microamps) that integrating a million lasers on a chip may become reality. This is still much less than the transistor count in a modern pentium, but if the memory and other "slow" functions are provided by electronics it would allow for the design of powerful processors.

Research reported by Hill at this conference [8] indicates that by using metallic cavities the size of lasers can become comparable with that of modern transistors. Due to their small size, these lasers would operate at very low powers, and their predicted operation speeds are well into the THz domain. Research on nanostructuring of materials and components should make it possible for these devices to operate at room temperature. Such lasers would pave the way for VLSI digital photonic ICs, containing millions of lasers, and operating at multi-TeraHz clock rates.

#### Integration Technologies

So far we have focused on InP-based integration technology, which is the obvious choice for complex circuits with a broad range of photonic functionalities: passive functions like coupling and filtering, signal generation, modulation, detection, and non-linear functions like wavelength conversion. It is the only technology that can support digital photonic VLSI.

For low-cost circuits with a low complexity level InP is a less obvious choice, however. For such applications silicon photonics, a rapidly emerging technology that uses mature CMOS-technology for fabrication of photonic ICs, is a promising candidate, and might become the dominant technology for circuits like low-cost transceivers for broadband access networks.

Both technologies use high-index semiconductors as waveguide material. High index waveguides allow for very small device dimensions, but the propagation losses in these materials are relatively high. For functions like high-Q filtering and time delay much lower losses are required. In the future photonic landscape there is room, therefore, for a third technology based on low-loss dielectric waveguides with a lower index contrast.

Another advantage of dielectric waveguides is that they can also be used at wavelengths outside the telecom windows, for example in the visible region. This makes them suitable as a hybrid platform for integration of passive functions (such as filtering and time delay) with active semiconductor based functions, such as light generation and amplifica-

tion, from the visible to the infrared region. Further, because of their favourable fibre coupling properties, they might act as an intermediary between semiconductor PICs and fibres.

The photonic functionality described above should be integrated in a compact and low-cost manner with the electronic functions that are required in almost any application. Ultimately we will end, therefore, with a package in which photonic functions are intimately integrated with electronic functions. This will start with today's hybrid integration technology, become more and more compact using advanced 3D integration technologies, and develop towards a VLSI photonic layer which is heterogeneously integrated onto a CMOS wafer.

### Conclusion

After a long time of development and struggling with market economics, photonic integration is becoming commercial reality. Costs are still high, however, because no large scale low-cost manufacturing facilities are available. For complex analog photonic circuits to penetrate mass markets, convergence in technologies will be mandatory, and here InP-based technology is a powerful candidate. Most probably in a hybrid technology platform that combines the power of InP-based technology with the power of CMOS. Such a technology is the subject of a number of research projects today.

For low-cost devices with a limited complexity silicon photonics will become a viable alternative, because of its compatibility with mature CMOS technology. For high complexity, involving light generation and amplification, and strong non-linear functionality, InP-based technology has a better potential and for large scale digital photonics it has no real competitor.

However, digital photonics is a dream so far. And so is much of what has been presented here. Many major issues have to be solved yet, such as thermal issues, developing a massive photonic interconnect layer, and finding proper ways of making the digital photonic circuits uni-directional, which is not trivial because of the strong preference of photonic circuits for reciprocal operation. But is a fascinating dream, and one that may come true.

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