Deep etched DBR gratings in InP for photonic integrated circuits

B. Docter, E.J. Geluk, F. Karouta and M.K. Smit

COBRA Inter-University Research Institute on Communication Technology
Eindhoven University of Technology
Faculty of Electrical Engineering, Opto-Electronic Devices Group
P.O.Box 513, 5600 MB Eindhoven, The Netherlands
Email: b.docter@tue.nl

Abstract: *A novel fabrication process for the realization of deep-etched DBR gratings in InP is presented. It is shown that a combination of chromium and SiO_x provides a very resistant etching mask for Cl_2-based ICP etching. Both e-beam and optical lithography are used to limit e-beam writing time.*

Introduction

Deep etched distributed Bragg reflector (DBR) gratings are very promising devices for InP/InGaAsP-based photonic integrated circuits (PICs). In theory, a first order deep etched grating can achieve a reflectivity of more than 97%, within only a few grating periods [1]. The small size and high reflectivity makes the DBR grating an ideal building block for high-Q cavities [2]. These can be used to make ultra small, in-plane lasers that can be applied in photonic logical circuits.

The realization of these sub-micrometer scale structures is very challenging. Being able to integrate the DBR mirrors with other photonic components adds additional restrictions to the fabrication process. We present here first results of a technology for fabrication of high quality 3 µm deep DBR gratings, using electron beam lithography and inductively coupled plasma (ICP) etching, which is compatible with our conven-tional Active Passive integration Technology [3].

DBR grating design

The first order DBR gratings are schematically shown in fig. 1. The air gaps in the DBR sections are about 390 nm wide and the lines are about 120 nm wide. This corresponds to ¼ of the wavelength in each medium. The p-InP cladding layer is sufficiently thick to avoid optical loss from the InGaAsP contact layer, which is necessary to integrate semiconductor optical amplifiers (SOAs) and optical phase shifters in the same chip. Because the gratings should be etched through the waveguide layer, an etch depth of at least 3 µm is required. Furthermore, the sidewalls should be smooth and vertical.

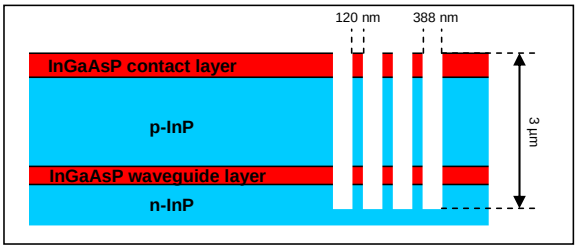

Fig. 1: *Schematic drawing of deep-etched DBR grating*

Fabrication process

To meet the above requirements a Cl_2:Ar:H_2 ICP process was used. This process has a high etch rate (~2.0 µm/min) and the addition of H_2 results in good passivation of the sidewalls. The selectivity towards a PECVD deposited SiO_x mask layer is about 20:1. However, because of faceting effects on the mask, which play a major role in the small DBR structures, this SiO_x layer needs to be at least 400 nm thick.

The grating structures are written using a Raith-150 electron beam lithography system, operating at 30 kV acceleration voltage. The typical thickness of common ZEP resist is 320 nm, which is not sufficient to accurately transfer a detailed pattern to the thick SiO_x layer, and therefore an extra 50 nm chromium mask layer was added.

The process flow is shown in fig. 2. The InP layerstack is covered by a 400 nm thick SiO_x layer by PECVD at 300 degrees. Subsequently a 50 nm thick chromium layer is evaporated and a 320 nm thick ZEP layer is spun on top. The ZEP resist is patterned using the e-beam lithography system. Usually a thin gold layer is deposited on top of the ZEP layer to avoid charging of the sample during e-beam patterning, but because of the chromium layer, this extra step is not necessary.

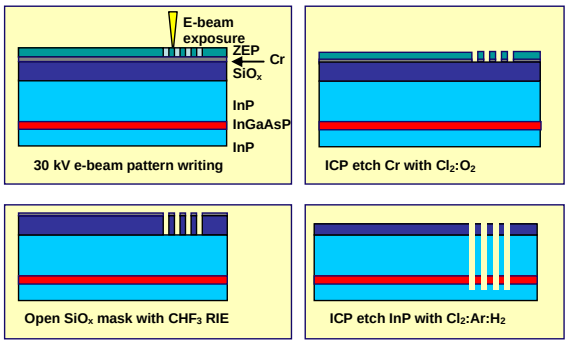

Fig. 2: *Process flow for the ICP deep etched DBR gratings*

After development of the ZEP pattern, the chromium is etched in an ICP system. A Cl_2:O_2-based process is used at intermediate ICP power and low RF power. This is a well known process that is also used for the fabrication of high quality photolithography masks [4]. The selectivity of the process is not extremely high (about 1:2 for Cr:ZEP), but it has a high uniformity, and since the chromium layer is very thin, this is an acceptable value.

Subsequently the chromium is used as an etching mask to open the SiO_x layer in a CHF_3 RIE process. The selectivity between chromium and SiO_x is approximately 1:17. This allows the thick-ness of the SiO_x layer to be well over 400 nm.

The high quality SiO_x pattern is used as a mask in a high power ICP etching process. The resulting DBR grating is shown in fig. 3. The ICP power was 1000 W and the RF power was 120 W. This gives very straight and smooth sidewalls. The roughness that is still visible on the DBR sections is caused by a sub-optimal proximity effect correction in the e-beam patterning.

Combination EBL - waveguide lithography

In the previous section a general process for fabricating deep-etched DBR gratings was presented. The process relies on EBL patterning of the full structure, and since ZEP is a positive e-beam resist, this requires writing the pattern around the DBR gratings and the waveguides. This means that if the DBRs are integrated in a bigger chip design, the total writing time becomes very long. Additionally, the proximity effect correction algorithm, which was originally developed for periodic photonic crystal structures, is not very suitable for these patterns. Therefore a more complex process was developed that enables us to define only the DBR sections by EBL and the rest of the waveguide structures by conventional lithography.

The process flow is schematically shown in figure 4. First the ZEP layer is patterned by EBL, defining the gaps between the DBR sections (fig 4a). The vertical lines are several microns wider than

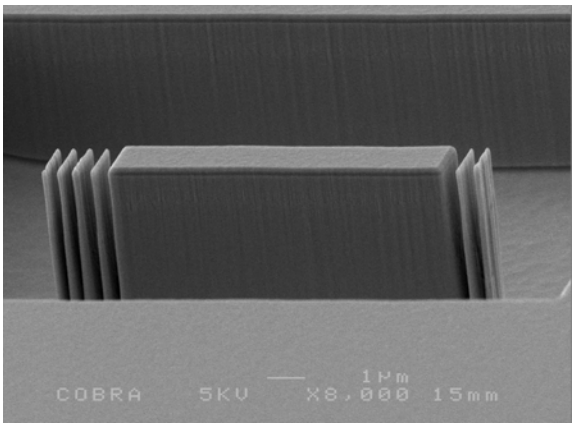

Fig. 3: *6 µm deep DBR gratings in InP*

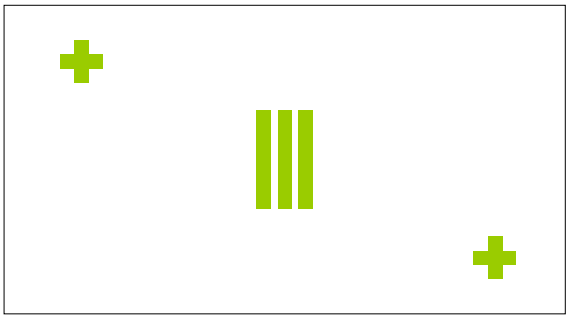

Fig. 4a: *EBL pattern*

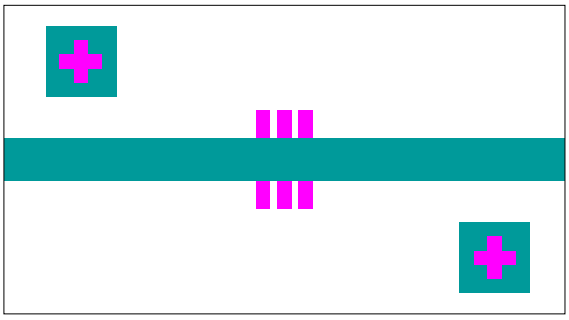

Fig. 4b: *Waveguide pattern aligned to EBL pattern*

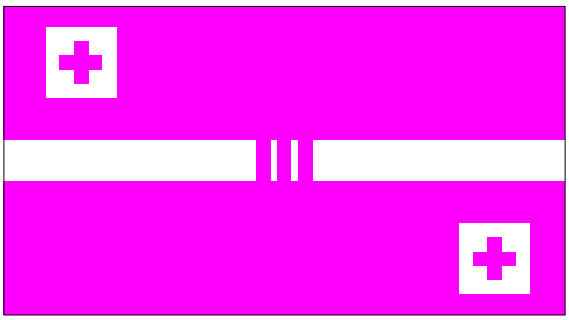

Fig. 4c: *Final chrome mask*

the waveguide, to compensate for lithography alignment errors. Together with the DBRs, alignment markers are written for the waveguide lithography step. Then the ZEP pattern is transferred into the chrome layer with the first ICP etch.

Next, the waveguides are defined by optical lithography (fig 4b). The pattern is aligned on the

markers defined in the chrome layer. A second chrome ICP etch is performed (fig 4c) after which the SiO_x etch and the InP etch are done.
This process has the advantage of being very accurate at the DBR sections, but requires less EBL writing time and is much more suitable for the proximity effect algorithm, since the EBL pattern is periodic. Also, the alignment of the two lithography steps is not very critical, because the DBR spaces can be made several micrometers wider that the waveguide.

Conclusion

We presented a novel fabrication process for deep etched DBR gratings in InP. The process is capable of realizing high quality deep etched structures with minimum EBL writing time. Furthermore, the technology is fully compatible with other processing steps and therefore enables the use of deep etched DBR gratings as building blocks in future advanced photonic integrated circuits. The first DBR gratings in passive waveguide structures are currently being realized using this new process technology.

References

[1] K.J. Kasunic, “Design Equations for the Reflectivity of Deep-Etch Distributed Bragg Reflector Gratings”, J. of Lightwave Techn., Vol. 18, No. 3, 2000

[2] T. Baba et al., “A Novel Short-Cavity Laser with Deep-Grating Distributed Bragg Reflectors”, Jpn. J. Appl. Phys., Vol. 35, 1996

[3] J.H. Den Besten et al. “An integrated 4x4-channel multi-wavelength laser on InP”, IEEE Phot. Techn. Lett., Vol. 15, nr. 3, 2003

[4] K.H. Smith et al. “Cr absorber etch process for extreme ultraviolet lithography mask fabrication”, J. Vac. Sci. Technol. B, Vol. 19, nr. 6, Nov/Dec 2001