Optimized Deep UV hardbake process for metal-free dry-etching of integrated optical devices

Gabriel Sengo, Henk A.G.M. van Wolferen, Kerstin Wörhoff and Alfred Driessen
Integrated Optical Micro Systems, MESA+ Research Institute; University of Twente
P.O. Box 217, 7500 AE Enschede, The Netherlands, E-mail: g.sengo@utwente.nl

Abstract: *Photostabilization is a widely used post lithographic resist treatment process, which allows hardening the resist profile in order to maintain critical dimensions and to increase selectivity in subsequent process steps such as reactive ion etching. In this paper we present the optimization of Deep UV-curing of 0,3-3.5 μm thick positive resist profiles followed by heat treatment up to 280 ^{0}C. The effectiveness of this resist treatment allows for metal mask free reactive ion etching with selectivity up to 6 for silicon structures, thermal silicon oxide and silicon oxynitride. A number of experimental results on integrated optics structures are presented that demonstrate the improved etch profiles obtained with this approach.*

Introduction

Positive photo resist is not only widely used as a mask for patterning structures in the semiconductor industry but also for manufacturing of a wide range of optical devices. In contrast to electronic devices, where many patterning steps involve small lateral dimensions in combination with a small step height, the main challenge in the patterning of optical devices consists in the high lateral resolution together with often a large step height. In our research group a large variety of optical devices based on Si, Si_3N_4, SiO_2 and SiO_xN_y waveguides have been designed, realized and tested.[1,2] For optical waveguide fabrication, the majority of those applications require a steep, vertical step which can be up to several microns high. In order to realize low-loss optical waveguides, side walls with low roughness are crucial. When applying reactive ion etching (RIE) on standard processed resist structures, the imposed ion bombardment often causes damage to the resist profile resulting in increased sidewall roughness. In addition, when exceeding the glass transition temperature (Tg) of the resist; re-flown masking material will inhibit the maintenance of dimensions.

Although process optimization was shown to result in well-defined, high quality waveguides, the processing and design windows become rather limited. Therefore in many fabrication schemes an additional metal hard mask was introduced, which solved the selectivity problem on one hand, but yielded new problems on the other side. In addition to loss-increasing metal contamination and rough side-walls, mask material erosion and redeposition causes the formation of "spikes"[2] (see Fig. 1) which also contribute to increased losses.

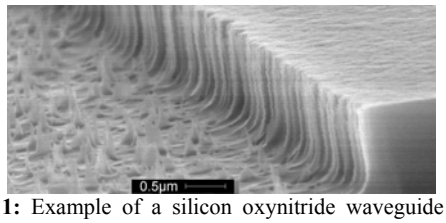

Fig. 1: Example of a silicon oxynitride waveguide with large side-wall roughness and spikes, typically obtained with an Ni hard mask in combination with RIE

Therefore, the application of metal hard masks should be avoided in low-loss optical waveguide fabrication and the feasibility of special resist treatment should be explored. The use of non-treated resist provides, however, also no solution, since most positive resist consist of novolac resins that begin to flow, depending on the manufacturer, at temperatures around 120^{0}C resulting in loss of critical dimension.
In order to make the resist structure thermally stable and strong so that it can withstand high temperatures which occur during the RIE and Ion Implantation, several resist treatment methods have been proposed. These include Deep UV (DUV) hardening followed by -or in combination with heating[3,4,5], plasma resist stabilization technique[6], and photoresist polymerization through pulsed photomagnetic curing[7]. In addition, hard baking of the resist structure at high temperature is also necessary to increase the resist selectivity during RIE.
Of the proposed resist treatment methods, DUV-curing and thermal heating is a widely used post lithographic process, to harden the resist profile in order to maintain critical dimensions and increase the resist selectivity necessary during the subsequent process steps such as RIE and ion implantation. In the following we apply this method to several integrated optics structures with critical dimensions.

Experiments

The experiments were carried out on various layer structures as used in integrated optics applications. The layers include blank silicon wafers, SiO_2 obtained by wet oxidization of Si-wafers or by plasma enhanced chemical vapor deposition (PECVD), low pressure CVD of Si_3N_4 and PECVD silicon oxynitride (SiON) of various thicknesses. The resist types used were the positive resist OIR 907/12, OIR 907/17 and OIR 908/35 of Arch Chemicals. After standard cleaning and resist spinning, the wafers were exposed with the Electronic Visions EV620 Mask aligner with a 12 mW/mm^2 conventional G-line (436 nm) light source. Different laser written masks were used with amongst others

waveguide structures of various dimensions, ranging from 0.9 to 4 μm. For the photonic crystals and gratings OIR 907/12 was diluted to obtain a thickness of 300 nm. The resist was then single exposed by a Laser Interference Lithography (LIL) system (λ=266 nm) for the gratings and double exposed for the photonic pillars. The grating period was about 500 nm.
For microring resonators OIR 907/12 was diluted to obtain thickness of 500nm.
After development, the wafers were, in contrast to the standard DUV-curing process carried out mostly in nitrogen or oxygen atmosphere[8], first intensely irradiated in an air filled chamber after which they were baked at temperatures of 180-280 ^{0}C for 1-3 hours.
After DUV-curing and a hardbake step, the structures were etched in Elektrotech Twin System PF 340 Reactive Ion Etching, Plasmatherm 790 parallel plate Reactive Ion Etching or Alcatel Adixen DE Inductive Coupled Plasma machines. The profiles were measured with a Dektak 8 of the Digital Instrument Veeco Metrology Group and examined with the Scanning Electron Microscope of JEOL, type JSM-5610/5610LV.

Results and discussion
The success of the photostabilization process strongly depends on the optimization of the two decisive processing steps, namely the heating and irradiation. It is believed that upon intense irradiation, a cross-linked outer skin of 100-200 nm with a higher degree of polymerization is formed. This skin should be strong enough to prevent the deformation of the resist profile even when hardbaked at elevated temperature far beyond the T_g of the resist. [3]
If the irradiation is not performed well, the internal stress due to heating or softening of the material above T_g might cause the deformation of the resist profile. On the other hand if the heating process is not carried out properly or too fast, the core of the resist profile will not have enough time to outgas and to harden resulting in deformation of the structure.

1. Process optimization for resist 907/17
In Fig. 2 the process optimization is presented for resist 907/17, spun at 6000 rpm, which gives a thickness of 1.2 μm.

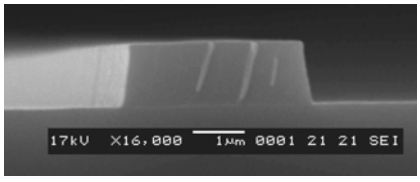

Fig. 2 (a): A typical resist profile after development in the OPD4262 positive resist developer.

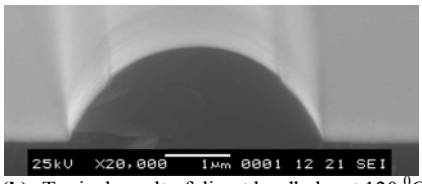

Fig 2 (b): Typical result of direct hardbake at 120 ^{0}C for 30 minutes without DUV irradiation. The T_g of the resist is exceeded causing severe reflow of the profile.

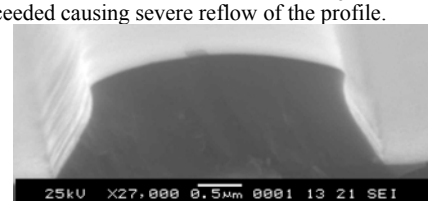

Fig. 2 (c): Not-optimized DUV-curing and direct hardbake at120 ^{0}C for 30 minutes. The outer-skin is too weak to withstand the internal stress.

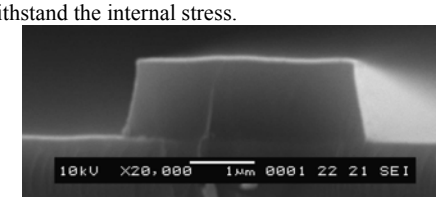

Fig. 2 (d): Optimized DUV-curing by applying proper irradiation time, followed by optimized hardbake with a final step at 120^{0}C for 30 minutes.

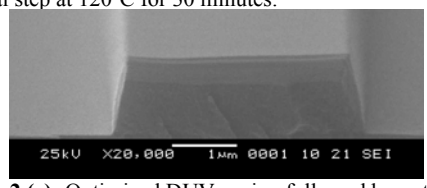

Fig. 2 (e): Optimized DUV-curing followed by optimized hardbake at 250^{0}C for 2 hours

The optimization of DUV- curing is obtained by the variation of irradiation time and optimization of the hardbake. The latter is done by performing bake steps with increasing temperature and by variation of the duration of those steps.

Starting with Fig. 2 (a), a typical resist structure after lithography without heat treatment is given. Fig. 2 (b) shows the result of hardbaking without applying DUV- curing. Fig. 2 (c) shows the importance of both the proper irradiation and gradual temperature rise in several steps. The irradiation is too short to form a strong cross-linked outer-skin to withstand elevated temperatures above T_g, resulting in the reflow of the profile. The next figures show the result of optimized temperature and irradiation. After achieving the optimized resist profile of Fig. (d), the result of (e) was obtained by further hardbaking steps up to 280^{0}C with an additional temperature optimization.

2. Process optimization for resist 908/35
In Fig. 3 the process optimization is presented for resist 908/35, spun at 4000 rpm, which gives a thickness of 3.5 μm.

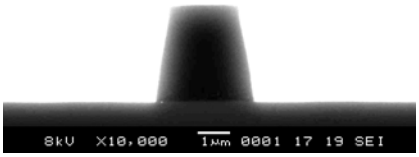

Fig. 3 (a): Typical resist profile after development.

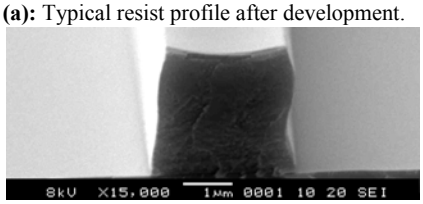

Fig. 3 (b): Similar resist profile with optimized DUV-curing followed by rampant heating from 25-180 ^{0}C for 3 hours.

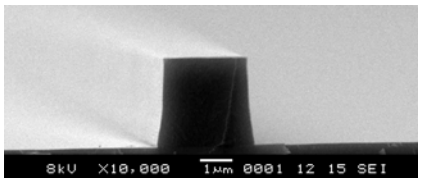

Fig. 3 (c): Optimized DUV-curing followed by optimized hardbake at 180 ^{0}C for 2 hours for the same profile.

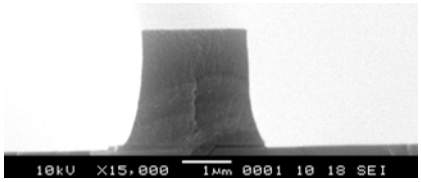

Fig. 3 (d): Optimized DUV-curing followed by optimized hardbake at 280 ^{0}C for 1 hour.

The set of figures show clearly the importance of controlled hardbake. If, after development (Fig. 3 (a)) the hardbake is carried out too fast, the internal stress will increase, resulting in the forming of the "wave" pattern of Fig. 3 (b). However, due to optimized DUV- irradiation, in analogy to Fig. 2, the cross-linked outer-skin prevents the reflow of the resist profile, see Fig. 3 (c).
After the optimization of both, the hardbake and DUV- irradiation, the resist has been baked up to 280 ^{0}C. As can be seen from Fig. 3 (d), the integrity of the profile is still well maintained, although the forming of the so-called "foot" is clearly present. This behavior was also observed by resist 907/12 and 907/17 baked at 280^{0}C. It appears that the bottom of the profile is slightly broader than the top which is of course partly inherent to the lithographic process, as can be seen in Figs. 2 (a) and 3 (a). The difference between the width at the top and bottom is varying from 0,15- 0.8 µm. The behavior of the "foot" is also clearly observed by I. Pollentier et al.[9]
To avoid the forming of the "foot", it is necessary to apply the hardbake below 280^{0}C. For our applications, the resist structures were used after an optimized hardbake at 180^{0}C for 2 hours.
The hardbake should be carried out step by step to the final temperature of 180^{0}C or higher in order to maintain the integrity of the resist profile.
Obviously the thicker the resist, the longer the irradiation and also a proper optimization is required. Characterizing and determining the proper sequence of DUV exposure and thermal rise to a final temperature are paramount to the success of photostabilization[8].

3. Diluted resist: nanostructures

For nanostructures as for example gratings, photonic pillars and microring resonators[10], thin resist is required to achieve high resolution in lithography. For this purpose resist 907/12 was diluted to obtain the thickness of 300 and 500 nm.

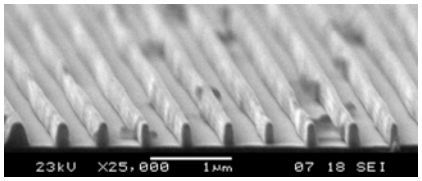

Fig. 4 (a): 300 nm optimized DUV-cured resist profile followed by optimized hardbake at 180^{0}C for 2 hours. This kind of resist structures has been used to etch gratings and photonic pillars.

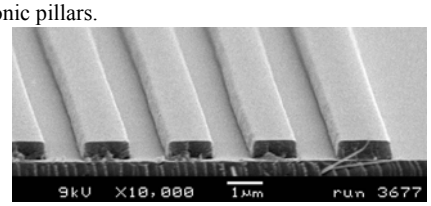

Fig. 4 (b): 500 nm optimized DUV-cured resist profile followed by optimized hardbake at 180^{0}C for 2 hours used for etching of microring resonators with a gap of 0,6 µm.

Figs. 4 (a) and (b) are typical resist structures used for etching of nanostructures in materials such as SiON, SiO2, Si3N4 and Si.
Compared to the resist structures of Figs. 2 and 3, the structures of figure 4 are obviously much shorter irradiated, because the thinner the resist, the shorter the irradiation time. The optimized hardbake was in all cases the same.

4. Etch selectivity

Experiments have been carried out with resist baked at 180 and 280^{0}C to investigate the etch selectivity. There was no noticeable difference measured between resist baked at these two temperatures. Therefore, for the further experiments, the resist profiles had an optimized hardbake with a final temperature step at 180^{0}C for 2 hours.
For PECVD SiON layers of 1.5 -2.5 µm deposited on silicon and etched in the Plasmatherm 790 dry etching machine, a selectivity of 5 was obtained. For layers of 1.5 -2.5 µm SiON deposited on 8 µm thermal oxide a selectivity of 6 was obtained. For silicon a selectivity of 4-5 is obtained for etching controlled structures of 200 - 1000 nm in the PF 340 Reactive Ion Etching twin system. For oxide, a

selectivity of 4 was obtained in the Plasmatherm 790 and a selectivity of 6 was obtained in the Alcatel Adixen DE Inductive Coupled Plasma etching machine. In addition, the silicon nitride selectivity never has been a problem; it is quite high.

5. Optical structures

Initial experiments have been carried out with PECVD SiON layers ranging from 1.0- 2.5 µm, because from the lithographic point of view, SiON is the most difficult material in achieving high resolution and high etching steps. If the photostabilisation process could be optimized for SiON, other materials like oxide, nitride and silicon would form no problem.

Under specific conditions it is possible for conventional contact mask lithography with a source wavelength of 436 nm, to open gaps of 600 nm, for example between a waveguide and a laterally coupled microring resonator.

In figure 5 some examples of these critical optical structures are presented.

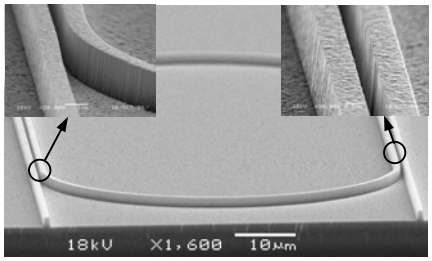

Fig. 5 (a): Microring resonator with a gap of 600 nm between the waveguide and the ring. The height is 1.7 µm etched in SiON layer of 2,5 µm deposited on 8 µm thermal oxide wafer.

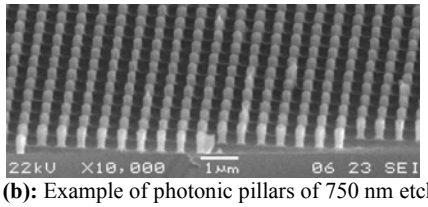

Fig. 5 (b): Example of photonic pillars of 750 nm etched in silicon using diluted resist of 300 nm obtained by LIL.

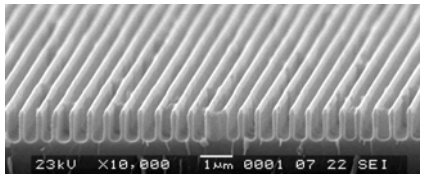

Fig. 5 (c): Example of gratings of 750 nm etched in silicon obtained by LIL using diluted resist of 300 nm.

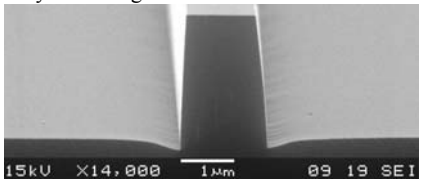

Fig. 5 (d): Waveguide of 2.3 µm height etched in thermal silicon oxide.

Fig. 5 (a) is a typical example of a microring resonator used for telecom applications obtained by SiON- technology using resist structures of Fig. 4 (b). Figs. 5 (b) and (c) are examples of respectively photonic pillars and gratings of 750 nm height etched in silicon using 300 nm hardbaked resist of Fig. 4 (a). Fig. 5 (d) is a typical example of a waveguide etched in thermal silicon oxide, with a sidewall angle of 85^0, obtained by Alcatel Inductive Plasma Coupled etching machine. With one micron harbaked resist, around 6 micron oxide can be etched.

Conclusion

It has been demonstrated that the use of the photostabilization process makes the resist strong and robust to withstand the subsequent process steps with minimum loss of critical dimension. The method is safe, clean, reliable, easy to apply and can be used for the production of wide range of critical optical devices in silicon, thermal silicon oxide, nitride and silicon oxynitride. In addition, the use of metal masks, causing a lot of problems in optical applications, for subsequent process steps can be avoided.

Acknowledgment

This work is partly funded by the Dutch National Broadband Photonics Access project.

References

1 K. Wörhoff et al., Electrochem. Soc. Proc., Vol. 2002-4, pp. 279-312, 2002
2 C. Roeloffzen, Ph.D. thesis, Enschede, 2002.
3 R. Allen et al., J. for Electrochem. Soc. vol. 129, pp. 1380, 1982.
4 R. Mohondro et al., Future Fab International, Vol. 3, pp. 235-247, 1997.
5 G. Jordhamo et al., International Society for Optical Engineering, Vol. 2724, pp. 588-600, 1996
6 W.H.L. Ma, International Society for Optical Engineering, Vol. 333, pp. 19-23, 1982.
7 Paul A. Ruggerio, Solid State Techn. Vol. March 1984, pp. 165-169, 1984
8 R. Mohondro, Solid State Techn. Vol. February 2003, 2003
9 I. Pollentier et al., Future Fab International, Vol. 12, 2002
10 D.J.W. Klunder et al., Appl. Phys. B, Vol. 73, pp.603-608, 2001