Comparison of optical passive integrated devices based on three materials for optical clock distribution

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Abstract: *We report different passive integrated devices characterization based on three materials (SOI, a-Si:H and SiNx) for the realization of an optical compact link compatible with CMOS technology. The low level of losses obtained on the passive elementary components for the optical link (strip guides, micro bend and MMI beam splitter) shows the feasibility of photonic integration on silicon using amorphous silicon.*

Introduction

With the increasing demand for high frequency operation and the size reduction of the integrated circuits, the ITRS predicts that the evolution of microelectronic technologies will meet important difficulties in the future [1]. One of the major limitations will come from the metallic interconnections due to delay of the signalling and high power consumption. One solution could be the use of optical interconnects for clock signal distributions [2]. First, different approaches used for the integration of an optical link are presented in this paper as well as material issues. The fabrication and measurement of the device are presented. Then, we give the results of the characterizations of the elementary components (strip guides, micro bend and MMI beam splitter). Finally summarize of this study will be done.

Different materials for optical interconnect

The integration of new optical functionality in a microelectronic process must be compatible with CMOS technology, which leads to two possible approaches of integration with specific advantages [3-4]. With the first approach (Frond-end), the passive optical components are fabricated at the same level than the transistors at the beginning of the IC process (figure 1). To meet integrated circuit performance requirements, Silicon-on-Insulator (SOI) substrates are now more and more used in microelectronics industry. It also is a powerful candidate for photonic integrated circuit. SOI is made of a thin silicon layer separated from the silicon substrate by a buried oxide layer (BOX). The large difference of refractive index (~2) between silicon and buried silica makes it possible to guide the light in silicon layer and to reduce the dimension of the integrated optical components to submicronic sizes compatible with the dimensions of the integrated circuits.

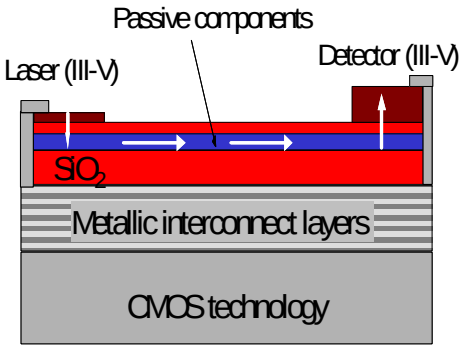

Figure 1 Diagram of integration of an optical link. The optical components are fabricated either on the top of the metal layers (Above IC approach), or at the level of components CMOS (Front end approach).

Using Front-end approach, the realization of various process steps is possible, but it requires an important modification at the level of the electronic design. So an alternative approach (above IC) can be envisioned, which consists in depositing a photonic layer above the integrated circuits at the end of the fabricating process (back end). Among the dielectric materials available in CMOS industry, Silicon nitride has the highest index of refraction that takes a better compromise between the density of the components and the design of the optical distribution. Also, it was grown by Plasma Enhanced Chemical Vapour Deposition (PECVD) at low temperature, that it makes it a good candidate for the integration of an optical link. In addition, in order to improve the compacity further, amorphous silicon (a-Si:H) photonical layer is studied whose index of refraction is larger than that of silicon nitride. The parameters of low temperature (<400°C) PECVD process were optimized to obtain photonic layer having possible higher index of refraction and lower level of losses of propagation losses in the infra-red domain.

Design, fabrication and measurement

Full vectorial mode solver [5] with transparent boundary condition [6] is used to perform the design

of the waveguide. This solver gives the propagation constant of the guided modes and it is also used to calculate the propagation losses due to leakage in silicon substrat. The modelling of 90° microbend is also simulated by Full vectorial mode solver with the conformal mapping method [7] to mimics the curvature of the waveguide. Geometries of the MMI splitters are evaluated by a 2D FDTD method coupled with the effective index method [8]. This method is less consuming in time and memory than a 3D FDTD and leads to the same results as regards with the devices optimization. The 3D FDTD is only used for results validation and for the computation of the losses of the devices.

All components are fabricated at CEA/LETI plan based on a standard CMOS technology with 8" wafer. TEOS was used as a precursor for oxide deposition. We manufactured the components with Deep UV (248nm) lithography and RIE etching (HBr) process for the realization of the strip waveguide. A cap layer of silica is added by PECVD process to encapsulate the optical circuit. An example of realization of strip waveguide of SiNx material is given on figure 2. In order to measure the index of refraction and intrinsic optical guided losses of the materials during process, a prism coupling technique (METRICON) is used. The characteristics of materials are summarized in table 1.

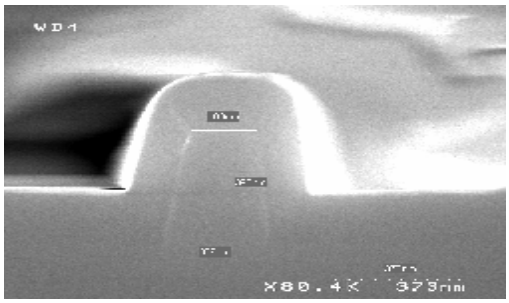

Figure 2 Cross-section of a strip guide of material SiN_x.

	SOI	a-Si:H	SiNx
Index at 1.3µm	3.505	3.4	2.1
Losses (dB/cm)	Non measurable	0.5	0.5

Table 1 The index of refraction and the intrinsic losses of planar waveguide for the 3 different materials that are investigated. The depths of the cord layer are respectively of 200 nm for the SOI and the a-Si:H, and of 400nm for the SiNx.

In order to have the spectral response of the devices in a strip waveguide configuration, light of 4 SLED sources is injected on the test devices by a butt coupling method with a tapered fiber and a linear polariser in line to get TE or TM like polarization. Manual 3D nanoactuators control the fiber alignment. The spectral response is collected by an output tapered fibre coupled with a spectrum analyser. A linear infrared camera is used to observe the light which is diffracted at the rough side wall of the waveguide.

Characterization of the elementary components

In order to evaluate the propagation losses of strip waveguides, as well as the losses of the 90° microbends and the MMI beam splitter for a wavelength range wavelength from 1.25µm to 1.65µm, we study a serie of devices shown in figure 3. They present 2 arms at the output: the first arm being a reference waveguide and the second arm include the elementary component to be studied. The losses measurements are presented in figures 4,5and 6 respectively for the strip waveguide, the microbend and the beam splitter MMI.

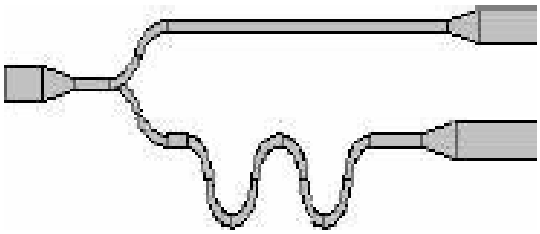

Figure 3 Devices for propagation losses measurements of waveguides and with the testing apparatuses.

For the sake of keeping the single mode condition in the components, we optimize the dimension of waveguide profile to $0.5*0.2\mu m^2$, $0.5*0.2\mu m^2$, $0.8*0.4\mu m^2$ for SOI, a-Si:H, SiNx. The losses at 1.3µm and 1.55µm are summarized in table 2. We report that the SOI and SiNx waveguides have weak losses of 2.9dB/cm and 2.2dB/cm at the wavelength of 1.5µm and 1.3µm respectively, which represents lowest level of propagation losses for strip waveguide encapsulated with PECVD silicon oxide [9] (see figure4). The losses of the a-Si:H waveguide are close to those of SOI crystalline material except for 1.375µm where the curve presents an absorption peak related to the SiOH bond in material. An annealing at low temperature (350°C) in the flow of hydrogen during 6 hours makes it possible to reduce considerably the influence of this absoption peak [10].

	SOI	a-Si:H	SiNx
1.3µm (dB/cm)	5.5	5.5	2.2
1.55µm (dB/cm)	4	4.5	6

Table 2 The propagation losses of strip waveguide for the three different materials at the wavelength of 1.3µm and 1.55µm.

We have tested the 90° microbends with different radii for SOI (2, 5, 10µm), a-Si:H (2, 5, 10µm) and SiNx (10, 15, 30µm). It is well know that the microbend losses decrease when the radius increase.

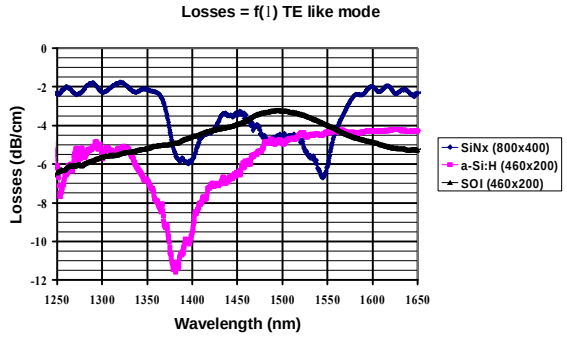

Figure 4 Evolution of the losses versus the wavelength for the strip waveguide.

An upper value of 0.15dB/bend has been taken, leading to a good compromise between the losses and the requirement of integration. We found an optimum radii value of 5µm for SOI and a-Si:H bends, and 15µm for SiNx (see figure5).

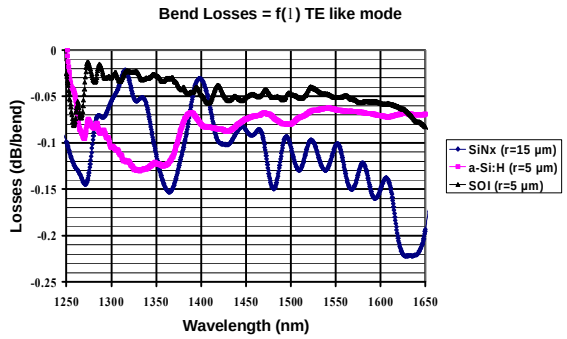

Figure 5 Evolution of the losses versus the wavelength for the microbends.

The characterizations of MMI beam splitter were realized with the same type of test device. The sizes are $2*5.4\mu m^2$ (SOI and a-Si:H) and $2.5*5.5\mu m^2$ (SiNx) and the excessive losses of MMI are 0.2dB, 1.3dB and 0.7dB for SOI, s-Si:H and SiNx respectively at the wavelength 1.3µm that is used for the design. The 3dB spectral ranges are 500nm for the SOI, a-Si:H device and are 250nm for SiNx device.

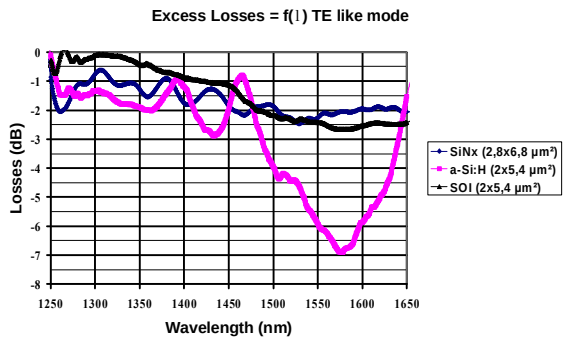

Figure 6 Evolution of the losses versus the wavelength for 1 by 2 MMI beam splitter.

According to the measurement of the elementary components, the passive optical distribution using different materials are realized. An example of a distribution from 1 entry to 8 exit including 7 MMI and 28 microbends for 1cm propagation distance is given on figure 7. The excessive losses for each branch are 6.28dB, 10dB, 4.66dB for SOI, a-Si:H, SiNx respectively. At the same time, the unbalance of each branch is ±0.5dB for the spectral range of the wavelength from 1300nm to 1600nm (figure 8).

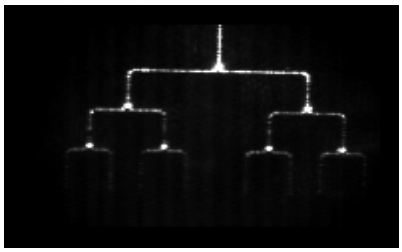

Figure 7 Optical distribution devices with measurements of spectral response of the elementary components.

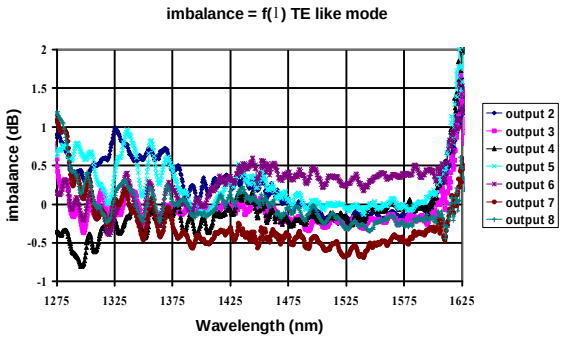

Figure 8 Unbalance of 8 exits in optical distribution.

Conclusion

In this paper we have studied three material approaches to optical interconnect: SOI, a-Si:H and SiNx. We have obtained results at the international state of the art on SOI devices (5dB/cm losses for $0.5*0.2\mu m^2$ waveguide at 1.3µm). Concerning a-Si:H and SiNx results, the value obtained (5.5 and 2.2 dB/cm) make them very attractive for photonic application. Particular a-Si:H that is studied for the first time. In our case, amorphous silicon has the same performances as SOI material but at a lower cost. It is also possible to design multilevel structures using this material, paving the way to 3D optical integration.

Aknowledgment

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