

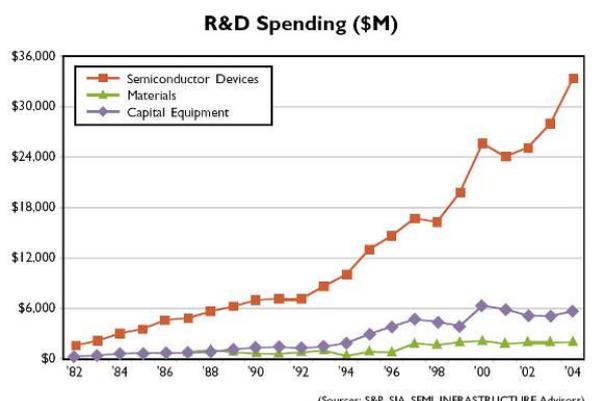
Trends in Silicon Photonics

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Abstract: Silicon photonics offers a compelling manufacturing and design platform to address today's imperatives for reducing the size, power, and cost of optical solutions. In addition to applications in telecom, the ability to provide low-cost photonics with integrated electronics may be enabling to many new applications in sensors and signal processing. This talk explores progress and potential in leveraging massive world-wide investments in silicon R&D into photonics applications, and examines outstanding challenges..

As mainstream CMOS technology contemplates 450mm wafers and ever-smaller feature sizes, the requisite R&D expenditures for process technology provide major challenges for silicon chip vendors. However, as seen in Fig. 1, even in 2004 the R&D expenditures for the silicon devices, materials and capital equipment exceeded \$40B annually.



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Figure 1. Annual R&D spend for devices, materials, and capital equipment in the silicon microelectronics industry. Even back in 2004 this had reached a level of over \$41B per year.

These investments offer an enticing opportunity for leveraging into photonics applications and markets. Key elements include (a) unprecedented film dimensional and compositional uniformity and reproducibility, (b) ultra-high resolution production lithography, (c) precision etch technology, and (d) exotic multi-layer metallization and other auxiliary features. These are all achieved without substantial optics-specific R&D, and immediately provide a pathway to high-volume manufacturing if designs can be realized that are compatible with mainstream electronics processing. From an optics perspective, silicon-on-insulator (SOI) in particular provides many attractive design attributes for photonic

circuits. Inherent physical benefits include a very high index contrast, enabling ultra-small bend radius index-guided circuits and devices[1], and a variety of high-performance photonic crystal concepts[2]. Examples of this are illustrated in Fig. 2 and Fig. 3 below, showing the work of Vlasov and co-workers at IBM[1].

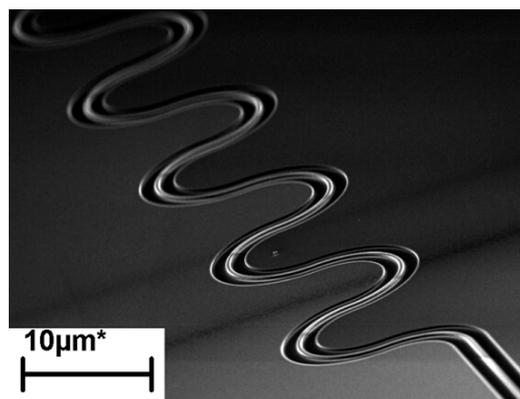


Figure 2. Demonstration of negligible bending losses in ultra-tight confinement SOI waveguides. Losses of 0.0043dB per turn were measured through a sequence of 200 turns with 6 μm radius[1].

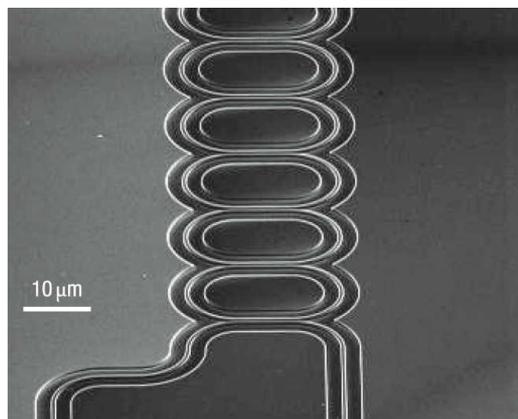


Figure 3. Ultracompact cascaded-ring slow-wave structure enabled by low-loss high-index contrast waveguide technology[1].

While silicon has historically not been viewed as a high-performance *active* optical material, recent work has now demonstrated that devices based upon plasma index mechanisms[3] can be quite efficient in field-effect configurations, effectively bypassing the previous bandwidth limitations of thermo-optic devices or forward-injection designs. Two designs have been explored, with results presented in the literature and recent conferences, and are

illustrated schematically below. The first utilizes reverse-biased P-N junctions, sweeping carriers in and out of the optical mode as the depletion region is minimized and maximized, while the second utilizes carrier accumulation (or depletion) in FET channels, which can be viewed simply as charge build-up at the gate oxide.

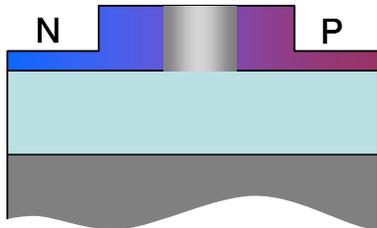


Fig. 4. Lateral P-N junction depletion-based modulator concept.

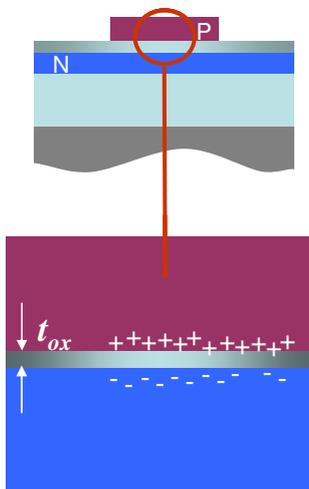


Fig. 5. Carrier accumulation at gate oxide.

Recent results on optical modulators include mm-scale Mach-Zehnder configurations from Intel[7] and Luxtera[6] with 10 Gb/s performance, and even 20 Gb/s devices from SiOptical[8]. With proper device design these modulators can be further reduced in size, but another path to small-area designs is through resonant enhancement[9]. Fig. 6 below shows an example of a highly compact ring configuration from Luxtera with sufficient modulation bandwidth for 10 Gb/s operation, while Fig. 7 illustrates a 20Gb/s Mach-Zehnder result from SiOptical, Inc.

Another promising Si-compatible modulation technology was recently demonstrated using the Quantum-Confined Stark Effect (QCSE) in Ge/SiGe quantum wells on silicon. InGaAsP QCSE electroabsorption modulators are a mainstay of today's telecom industry in the form of integrated laser modulators. As shown in Fig. 8, the performance of the Ge/SiGe device on silicon was comparable with standard InGaAsP designs,

suggesting that waveguide modulators with 100 μm scale lengths should be readily achievable.

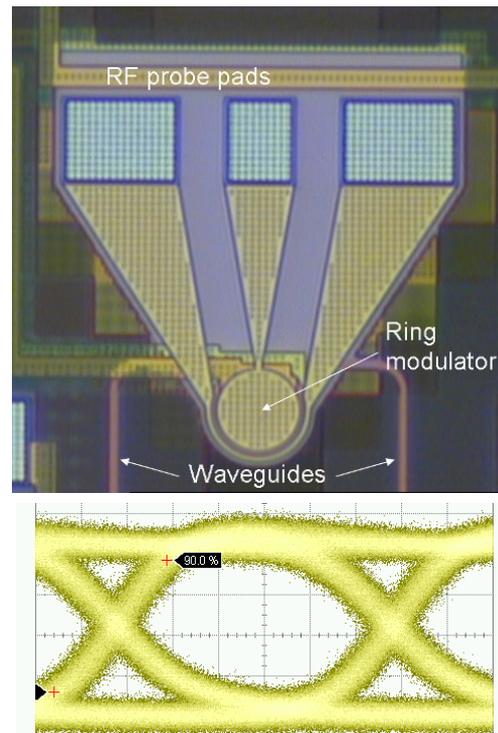


Fig. 6. Top: Compact resonant ring modulator from Luxtera[6] exhibiting open eye diagrams at 10 Gb/s (Bottom)

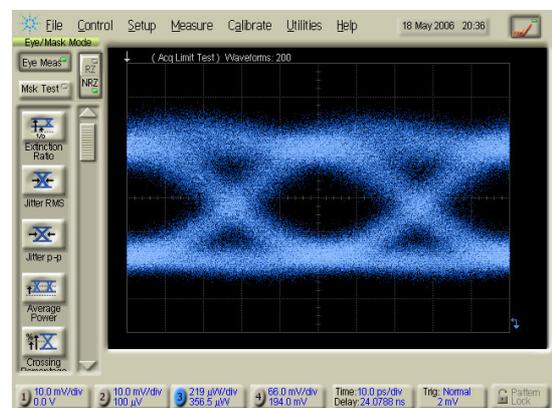


Fig. 7. 20 Gb/s eye diagram from SiOptical Mach-Zehnder modulator

Ge-based detectors, implemented with SiGe VLSI epitaxy technologies, have demonstrated high-performance waveguide designs and suggest that integration of photodetector function is not a major barrier.

The result of these studies is a nearly full suite of active and passive photonics devices that can be implemented with very high density and yield using commercial CMOS foundry technologies, with well-documented low costs per unit wafer area. In

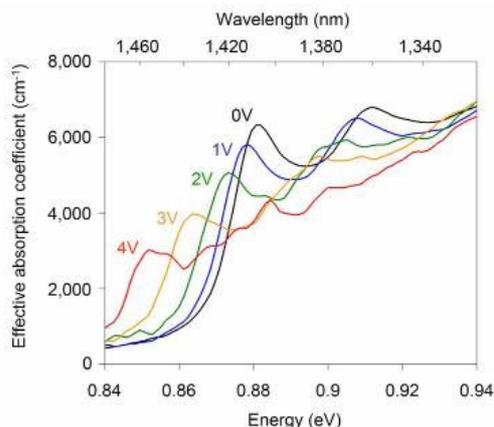


Fig. 8. QCSE modulation in Ge/SiGe quantum wells on silicon[9]

addition to broad progress in the international research community, there has been significant recent acceleration enabled by DARPA's EPIC program[5,6], as well as impressive advances from start-up companies pursuing product development or deployments in concert with major silicon foundry partners.

In addition to low cost, silicon photonics also offers potential for much lower electrical power consumption for optical links and interconnections. This results in part from the inherent voltage scaling that can be achieved through reduced dimensions in field-effect devices. An obvious benefit of designing into a CMOS foundry is the ability to integrate optical functions with standard VLSI circuitry functions on a single silicon chip. For example, Luxtera has demonstrated Mach-Zehnder modulators with integrated on-chip drivers at 10 Gb/s[6]. This integration can improve impedance issues compared to conventional multi-chip configurations for further potential power reduction. This is important especially in high-density array configurations, where additional power savings may be realized through sharing a single laser source for multiple communications ports.

Silicon photonics also offers promise for markets outside of telecom and data links, including sensors and signal processing applications, where the ability to integrate optical functions with advanced preamplification, DSP, and controller functions on a single low-cost chip could be dramatically enabling.

While these applications can and will proceed using off-chip optical sources, one outstanding challenge is a silicon-compatible electrically-pumped laser. This shortcoming will continue to make large-scale InP-based integration dominant for the highest performance core-network WDM-based applications[11]. However, recent progress has been

demonstrated in hybrid integration, both in the form of sophisticated flip-chip grating-based coupling of III-V lasers on silicon photonic chips, as well as more intimate wafer-bonded hybrid integration where the laser utilizes a predominantly silicon waveguide. This talk will review recent work towards silicon-compatible lasers, including intrinsic, extrinsic, and hybrid materials technologies.

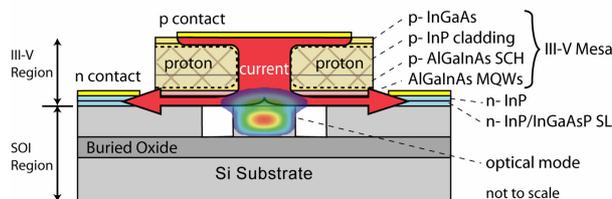


Fig. 9. Hybrid wafer-bonded III-V/Si laser demonstrating room-temperature, CW operation with 1.8 mW of fiber-coupled output power [12]

Acknowledgments

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