Amorphous Silicon in Nanophotonic Technology

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Abstract: Silicon-on-insulator nanowire waveguides appear to be the technology for next generation of super compact integrated devices. Due to a very high refractive index contrast and strong light confinement in the core, the waveguide bend radius can be reduced to a few micrometers and the size reduction of the functional integrated circuits can reach several orders of magnitude in comparison to standard integrated optics based on silica-on-silicon technology. Amorphous silicon is an interesting material allowing for more flexibility in nanowire structures. An array waveguide grating multi/demultiplexer that usually occupies several square centimetres in silica-on-silicon technology can be reduced to the size of 320 x 270 μm^2.

Introduction

Highly integrated photonic devices based on materials with high refractive index contrast gain more and more interest when the complexity of photonic structures increases and the integration of photonic and electronic circuits becomes a reality.

High refractive index contrast means strong light confinement in the waveguide core allowing for very small core sizes and sharp waveguide bends and leading to shrinkage of the component size by several orders of magnitude in comparison to traditional low contrast integrated optics.

There ares several possible material structures suitable for realizing complex photonic devices. Those ones, based on III-V semiconductors gained a lot of attention as it is possible to realize almost all important for optical communication building blocks in this technology: passive waveguides and wavelength selective devices, light sources, switches, modulators and detectors. However, for very small structures high index contrast to the air or dielectric overclading is not sufficient as light leaks out of the bends to the buffer or substrate because of the low index contrast between substrate and epitaxial grown materials. III-V semiconductor-based structures suffer also for higher losses and higher material cost. Moreover, their material technology is more complex in comparison to other technologies based on silicon wafer.

Silicon is an inexpensive material and the most widely used semiconductor material in current electronic devices. For photonic applications it is important that silicon has low losses for optical communication window and high refractive index of 3.5 in comparison to silica (n=1.5), which can be used as surrounding media for the light guiding waveguide core. Strong light confinement of such structures allows for very sharp bends and submicrometer core sizes and enables design of nano-scale optical devices and ultra-compact optoelectronic systems.

Additionally, silicon photonic devices can be fabricated using standard silicon processing technology. Compatibility with CMOS techniques allows cheap mass production of monolithically integrated optoelectronic structures.

Silicon components can play different wavelength selective functions and silicon waveguides can serve as connection links guiding optical signals among active and passive elements. Silicon, as an indirect semiconductor, has a very inefficient light emission at room temperature; therefore the active structures for photonics applications are usually based on the III-V materials and are usually not compatible with silicon. Recently a lot of effort is devoted to overcome these shortcomings of silicon.

SOI technology

Most of the fabricated passive nanophotonic devices are formed using silicon-on-insulator (SOI) technology. Here, commercially available SOI wafers are normally used, with thickness of the silica buffer and the top silicon layer optimized to get low leakage to the substrate as well as single mode light guiding at 1.55 μm. One of the commonly used standard SOI wafers has 1 μm silica buffer layer and 220 nm single crystalline high quality silicon layer [1].

With this technology sub-micrometer size waveguides – “nanowire waveguides” can be formed using e-beam or deep UV lithography and high precision plasma etching. Typical parameters of these waveguides are: core size 220 x 500 nm^2, bending radius below 5 μm, straight waveguide losses about 2 dB/cm and coupling losses of order of 7 dB/point, that can be considerably diminished using a specially designed tapers or mode converters.

Main limitation of SOI-based waveguide technology is lack of flexibility in design and material parameters. This flexibility can be offered by alternative technologies, where the different material layers are deposited during the technological process and can be customly adjusted depending on the demands.

Here we describe our optimized amorphous silicon technology that allows to freely adjust the deposited layers thickness and their refractive indices, and makes it possibile to fabricate more complex structures including multi-layer components, vertical cavities and Bragg reflectors [2, 3].

Hydrogenated amorphous silicon

Amorphous silicon is a known from long time ago semiconductor material mainly considered for applications in electronics [4] and solar cells [5]. Unhydrogenated amorphous silicon films, obtained most often by thermal evaporation, sputtering or ion bombardment contain usually a large amount of point defects in form of dangling bonds associated with silicon single- or multivacancy complexes within the disordered amorphous network [6]. These defects degrade electric performance of the semiconductor as well as generate absorption bands at the optical communication wavelengths between 1.3 and 1.6 μm.

Hydrogenated amorphous silicon (a-Si:H) was obtained for the first time in 1969 using glow discharge to generate plasma with silane (SiH_4) as a precoursor. This technique resulted in much lower concentration of dangling bonds, which were saturated by hydrogen atoms. The improvement of electrical parameters of this material as well as observed photovoltaic effect made it very interesting for applications to large area electronic arrays, displays, optical scanners and solar cells. Research was concentrated on the optoelectronic properties of a-Si:H in the visible part of spectrum for a long time, although recently scientists recognized its good optical properties in IR region for optical communication applications [7].

Presently to obtain good quality a-Si:H material for optical applications, Plasma Enhanced Chemical Vapor Deposition (PECVD) technique is commonly used with very low RF power at 13.56 MHz, which is essently the modified glow discharge technique used for the first a-Si:H deposition. Low power prevents ion bombardment that generates defects rather than assists the deposition. Relatively low temperature between 200 °C and 300°C and other process parameters are optimized to incorporate a right amout of hydrogen, that should passivate most of the dangling bonds, but the excess of hydrogen can increase the material porosity and increase scattering losses.

Here we use pure silane (SiH_4) as a gas precursor, RF power 10-20 W and 200 mTorr process pressure.

The low pressure and power levels prevent excessive polymerization of silane radicals in the gas phase. It contributes also to the low deposition rate, but as the film thickness necessary for fabricating waveguides is below 300nm it is of less importance. In Fig. 1 the deposition rate as a function of deposition temperature is shown for an RF power of 10W and 20W.

As it is seen from the graph, the deposition rate is very much dependent on the RF power. It facilitate to adjust this parameter together with silane flow rate to obtain the conditions, where the reacting molecules have short residence time in the chamber preventing unwanted polymerizing reactions in the gas phase.

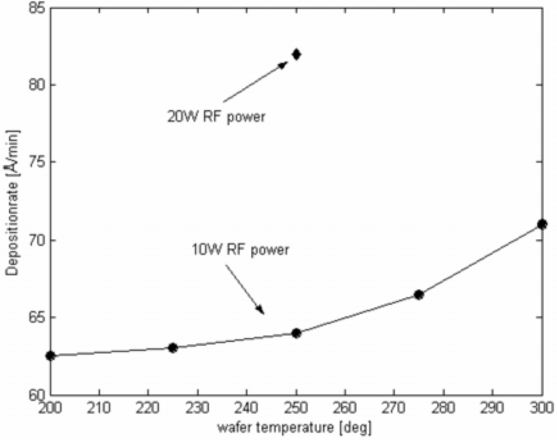

Fig. 1: Deposition rate as a function of the substrate temperature, at a process pressure of 200 mTorr.

The hydrogen can be incorporated into the films either singly, doubly or triply in SiH, SiH_2 or SiH_3 groups. Each of them has absorption bands at around 630 cm^{-1} and 2000 cm^{-1} as shown in Table 1.

Table 1: IR absorption peaks for three SiH_n groups

Group	Bond stretching	Bond bending/rocking
SiH	2000 cm^{-1}	630 cm^{-1}
SiH_2	2090 cm^{-1}	630 cm^{-1}
SiH_3	2140 cm^{-1}	630 cm^{-1}

The optimization of the processs parameters was towards formation of only SiH type of bonds in the film to increase film homogeneity. The ratio of SiH_2 and SiH_3 to SiH groups can be minimized by increasing the substrate temperature and reducing the silane pressure [6]. The absence of SiH_2 and SiH_3 groups was confirmed by taking a FTIR spectrum of prepared samples at around 2000 cm^{-1} and by measuring the correlation of the integrated absorption at 2000 cm^{-1} and at 630 cm^{-1}. FTIR spectrum for the samples with 500 nm a-Si:H film deposited with RF power 10 W, shown in Fig. 2, exhibit lack of absorption peaks characteristic for SiH_2 and SiH_3 groups. Fig. 3 plotted for the same samples shows strong correlation of the integrated absorption at 2000 cm^{-1} and at 630 cm^{-1}.

The optimization of temperature to obtain good quality a-Si:H films is quite complicated. As it was stated, with increasing the temperature the content of the SiH_2 and SiH_3 groups is decreasing, but also the total amount of hydrogen in the film falls down. To find the optimal deposition temperature the deposited material quality was evaluated directly by measurement of propagation loss in optical waveguides patterned on the fabricated samples. Strip loaded waveguides with geometry shown in Fig. 4 and cutback method for loss measurement were used.

The structure consists of 6 μm SiO_2 layer deposited on the silicon substrate, 0.22 μm thick layer of a-Si:H core and a top ridge of the waveguide, made of SiO_2.

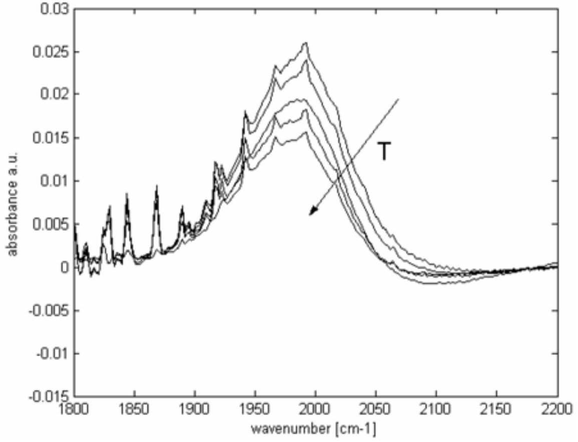

Fig. 2: FTIR spectrum of the a-Si:H film with only SiH band at 2000 cm^{-1} seen. Temperatures as in Fig. 1.

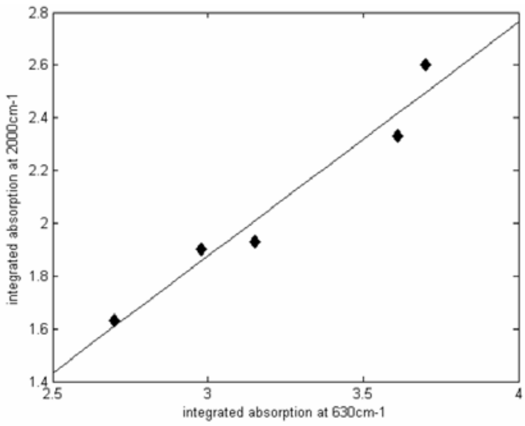

Fig. 3: Integrated absorption correlation between the 630 cm^{-1} and 2000 cm^{-1} bands for the same samples as shown in Fig. 2.

Fig. 4: Cross section of the waveguide structure used for measurements of the material losses.

The ridge is etched to be 3 μm wide and 0.45 μm thick, then there is 0.05 μm thick layer of SiO_2 left to cover underlying core.

According to the simulation this structure gives a single mode waveguiding with propagating light well confined in the a-Si:H layer just under the SiO_2 strip with confinement factor approx. 0.9. In this way we almost eliminated loss originating from surface roughness due to lithography and etching. The measured here loss is mostly due to material quality being tested. Fig. 5 shows the results measured for 1.55 μm. The propagation loss is constant with accuracy of +/-0.5dB within the band 1.52 μm to 1.62 μm of ASE unpolarized source used for measurements. The propagation loss of 1.5dB/cm for the temperature 250°C was measured, therefore this temperature was chosen as optimized deposition temperature for fabrication of amorphous silicon devices. The refractive index of the optimized a-Si:H at 1.55 μm was measured using spectroscopic ellipsometry to be 3.63.

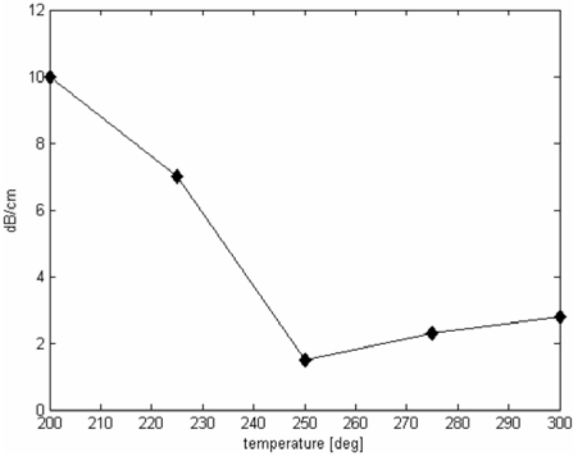

Fig. 5: Propagation loss in a-Si:H strip loaded waveguides, as a function of the deposition temperature.

Silicon nanowire waveguides and devices

5 μm silica buffer layer and 250 nm a-Si:H core layer patterned to 500 nm wide strips is the structure used here for fabrication of single mode nanowire waveguides and waveguide devices. A cross section of this structure is shown in Fig. 6.

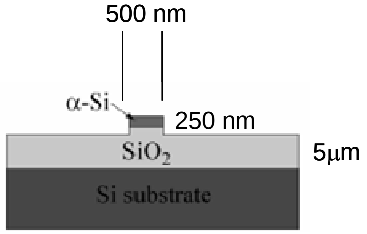

Fig. 6: Structure of the films and patterning used for single mode nanowire waveguides and waveguide devices.

In this technology both layers are deposited with Plasma Enhanced Chemical Vapor Deposition (PECVD), patterned by e-beam lithography and subsequently etched with Inductively Coupled Plasma Reactive Ion Etching.

In these sub-micron size structures the fabrication accuracy has a very critical influence on the performance of the devices. High contrast makes that waveguide losses are very sensitive to scattering at roughness on the core-cladding interface. Especially the sidewall surfaces after etching the waveguide profile are crucial for the final quality of the device. Both, lithography and etching itself can have influence on the sidewall roughness and so both these steps should be optimized. The sidewall roughness can be also improved after etching by slight thermal oxidation of the etched silicon profiles.

As an example for the Si nanowire waveguide components fabricated in amorphous silicon technology a compact arrayed waveguide grating (AWG) is fabricated.

An AWG with 1.6nm channel spacing and a layout of overlapped "free propagation regions" [8] is shown in Fig. 7. This novel layout introduces more flexibility for the design, and the separation between two adjacent arrayed waveguides can be further decreased. Consequently very compact AWG can be achieved. The detailed structural parameters for this AWG are presented in Table 2.

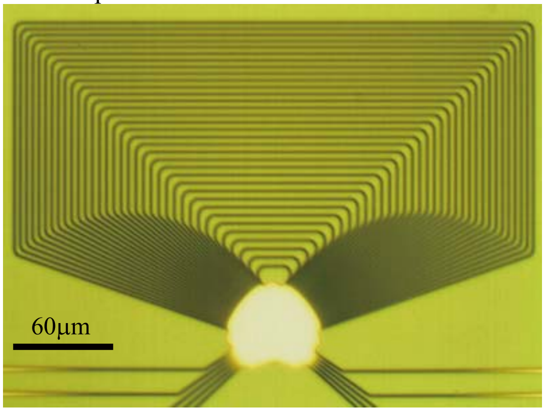

Fig. 7: Picture of the fabricated Si nanowires and AWG.

Table 2: Structural and measured parameters of the AWG.

Designed structural parameters	
waveguide dimension	500 x 250 nm^2
number of arrayed waveguides	34
number of channels	5 x 5
constant length difference ΔL	24.9 μm
diffraction order	42
FPR (focal) length	50 μm
output waveguide width at FPR	1.5 μm
output waveguide spacing at FPR	350 nm
arrayed waveguide width at FPR	950 nm
arrayed waveguide spacing at FPR	50 nm
total size	320 x 3270 μm^2
Measured spectral characteristics (TE polarization)	
channel spacing	1.5 nm
free spectral range	21.7 nm
insertion loss	~- 8.5 dB
Crosstalk	~-7dB

After the deposition the wafer was then cleaved into small samples. The Raith 150 EBL system was used for creating the patterns of Si nanowires and AWGs. To increase the coupling efficiency, the width of each input and output waveguide was tapered from 500nm to 2 μm through a 25 μm long linear taper. The samples were then etched using ICP-RIE with the SF_6 and C_4F_8 gas mixture. The roughness of the sidewall is ~10nm, which is directly measured from the SEM pictures.

Fabricated straight waveguides were measured with the end-fire characterization setup giving the propagation loss of ~4dB/mm using cut-back method. For photonic devices based on Si nanowires, such a loss level is still acceptable.

Fig. 8 shows the spectral responses of the fabricated AWG for the TE polarization. The measured spectral characteristics are listed in Table 2.

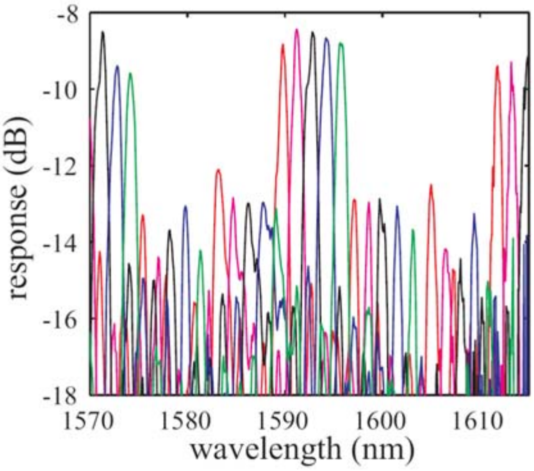

Fig. 7: TE spectral response of the AWG.

We can find that the crosstalk is relatively high here and we attribute this to the phase error induced in the arrayed waveguides due to the width variation in short range (sidewall roughness) and long range (stability of the E-beam during exposure). Due to the high confinement of light in Si nanowires, even a small change in width will cause a large variation in the propagation constant. Improving the fabrication process or introducing a tuning mechanism to each of the arrayed waveguides can decrease or compensate this phase error, and help to achieve a lower crosstalk.

Conclusions

Reduction of dimensions in future highly integrated photonic devices is due to application of materials with high refractive index contrast, where much higher light confinement allows for very small core sizes and sharp bends. Amorphous silicon is proposed as an alternative to SOI technology and used for fabrication of nanowire waveguide-based AWG .

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