Monolithic 2x2 Quantum Dot Switch for Optical Interconnect Networks

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Abstract: *The design, fabrication and performance of an integrated 2x2 Quantum Dot SOA based switch is reported. Low penalty performance and a large dynamic range opens the potential for the 2x2 switch to be cascaded as a building block for multi-stage, high capacity optical networks.*

Introduction

Recent studies of quantum dot (QD) semiconductor optical amplifiers (SOAs) have demonstrated properties of broad gain bandwidth, low noise performance, ultra-fast gain recovery, high saturation output power and low crosstalk performance [1-6]. These characteristics are of potential importance in a wide range of prospective applications such as power boosters, in-line repeaters, optical cross connects and optical add/drop multiplexers. The use of active components as add/drop multiplexers are of great interest because of their inherent gain, potentially removing the need for additional amplification in cascaded applications. However, the noise of such systems has limited their potential cascadability, even when using quantum well devices [7]. In this paper we report the operation of quantum dot components which have the potential for greater cascadability [5,6]. Following an investigation of the static performance and noise properties, a dynamic study is presented and the potential of the quantum dot switch for interconnect networks is discussed.

Device Details

The structure of the 2x2 QD switch is presented in Figure 1. It has an overall chip area of only 2.55x0.85 mm^2. The switch incorporates a QD active structure which is grown on a GaAs (100) substrate using molecular beam epitaxy. The active layer comprises a ten-fold stack of $In_{0.15}Ga_{0.85}As$ QDs, separated by 38nm GaAs buffer layer and embedded in a GaAs waveguide. The active layer is sandwiched between two $Al_{0.35}Ga_{0.65}$ layers which form the cladding layers. Standard photolithography and ICP dry etch processes are used to fabricate the ridge waveguide structures. Each of the four input ridge waveguides has a width of 3 µm which expands linearly to a 6 µm width, over a length of 150 µm, to the integrated beamsplitter, before connecting to perpendicular SOA gates. The integrated beamsplitters (see Figure 1 inset) contain a 45° totally internal reflecting (TIR) mirrors to route the light to the drop and through paths. The TIR mirrors are formed by focused ion beam etching vertical slots through the active layer. Patterned p-type electrodes allow individual addressing of the amplifier gates and splitters. The isolation between the electrodes exceeds 5kΩ for all electrode combinations.

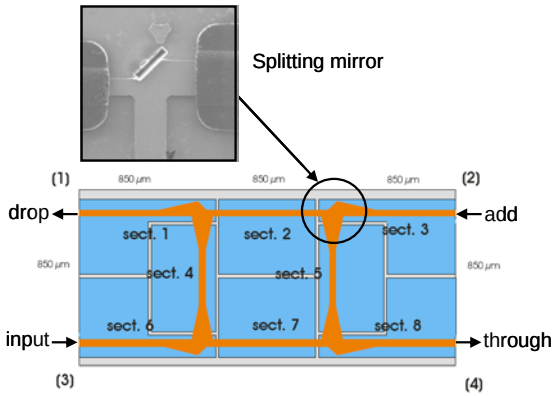

Fig. 1: Schematic of switch structure showing the inputs, outputs, waveguides, splitters and SOA sections. The totally internally reflecting mirror is shown as an inset.

As can be seen from Figure 1, there are eight individually addressable QD SOAs, each connected by the four integrated beamsplitters. The SOAs in sections 1,3,6,8 gate the I/O ports of the switch, while the SOAs in sections 2,3,7,8 gate the splitting stages within the switch. Through the use of an electronic control scheme, the switch operates on a broadcast and select basis to realise a full non-blocking 2x2 switching capability.

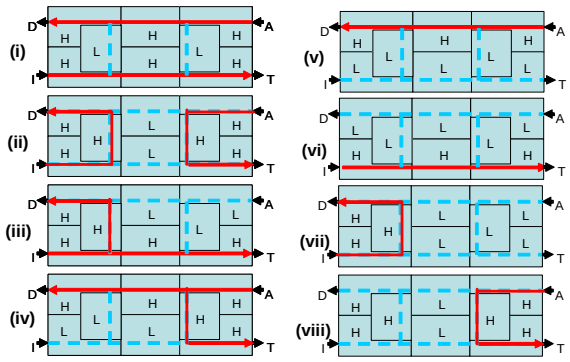

Fig. 2: Monolithic add drop multiplexer mode of operation. Switch bias levels for gates in section 1 to 8 as defined in Figure 1. Abbreviation: Input (I), Through (T), Add (A), Drop (D), On (H), OFF (L). The different operations are as follow: i) bar state (I to T, A to D), ii) cross state (I to D, A to T), iii) broadcast I (I to T and D), iv) broadcast A (A to T and D), and single mode operation: v) A to D, vi) I to T, vii) I to D, and viii) A to T

Mode of Operation

The combination of 'on' and 'off' SOAs for switch-

ing is shown in Figure 2. For the 'off' state a low bias current of less than 20mA is applied, such that the loss in the SOA gate will block any input signal from the 'add' or 'drop' ports, but will still allow fast switching to the 'on' state. For the 'on' state a bias current of between 50mA and 100mA can be applied to provide a net gain out of the SOA. Figure 2 presents the full range of add, drop and broadcast functionalities are avaialbe from this desing. Figure 3 demonstrates the switching operation of a data signal, where the input data is routed to the 'through' and 'drop' paths with the electronic control schemes shown in Figure 2 (vi) and (vii).

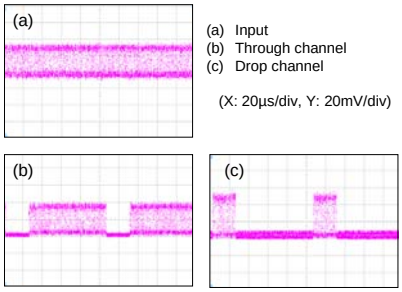

Fig. 3: Oscilloscope capture of 2x2 switch in switching application, showing data switching between the through and drop paths.

DC Characteristics

Continuous wave measurements have been carried out to investigate the DC characteristics of the 2x2 QD switch. Both the through and the drop channels have been investigated for gain saturation, power gain and noise figure. The gain saturation characteristics of the switch are measured for a drive current of 100mA and at a wavelength of 1290nm. The gain dependance on drive current is plotted for a wavelength of 1270nm with an input power of -15dBm, and the gain dependence on wavelength is plotted for a drive current of 100mA with the same input power. Noise figure measurements are performed by directly comparing the optical signal to noise ratio before and after the 2x2 switch. The coupling loss in these devices has been measured by the photocurrent technique to be 3.1dB. At 1290nm, gain saturation is found to occur at on-chip output powers of 6.8dB for the drop path and 10.5dB for the through path. The maximum peak on-chip gain, which occurs at a wavelength of 1275nm, is measured to be 12.1dB for the through path and 9.3dB for the drop path. The 2.8dB difference in on-chip gain between through and drop paths is attributed to the excess loss of the two TIR mirrors in the drop path (the low mirror loss being the result of optimisation of the offset of the mirror at the crosspoint). Minimum noise figures of 7.4dB for the through path and 8.0dB for the drop path are measured at a wavelength of 1275nm. Improved input and output coupling designs, such as expanded mode waveguides, are expected to reduce the system noise figures.

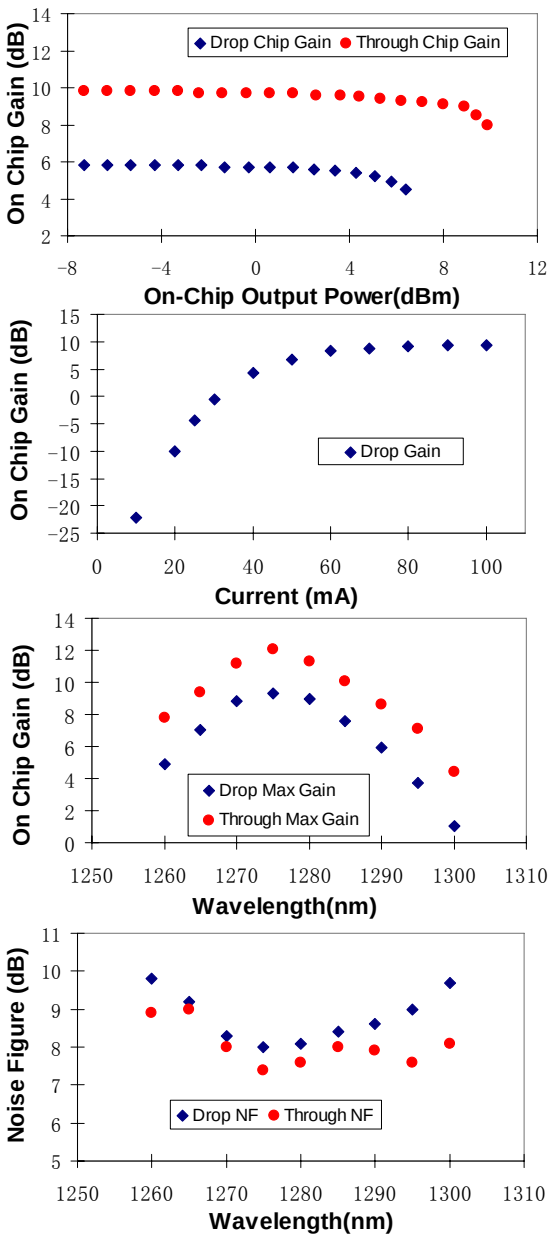

Fig. 4: (a) On-chip gain vs input power of the 2x2 switch at 1290nm, 100mA bias current. (b) Un-saturated on-chip gain vs drive current at 1270nm. (c) On-chip gain and (d) noise figure as the function of wavelength at a bias current of 100mA and -15dBm input power

Dynamic Operation

To investigate the dynamic operation of the 2x2 switch, a complete transmission and reception test-bed is constructed. The input into the switch is sourced by a single frequency laser of 1290nm wavelength, and is modulated at a data rate of 10Gb/s with a PRBS sequence of 2^{31}-1. As the current chip exhibits high polarization dependent gain (inexcess of 20dB), a polarization controller is used prior to the chip's input to ensure a TE input polarisation state. Isolators are used to prevent reflections into the SOAs while a filter is used before the receiver to filter the contributed amplified spontaneous noise from the amplifiers. A commercial multi-quantum

well SOA is placed before the receiver to provide the necessary power budget to perform the input power dynamics range (IPDR) measurement. The BER as a function of the switch input power for the 'through' and 'drop' paths is measured to characterise the dynamic performance.

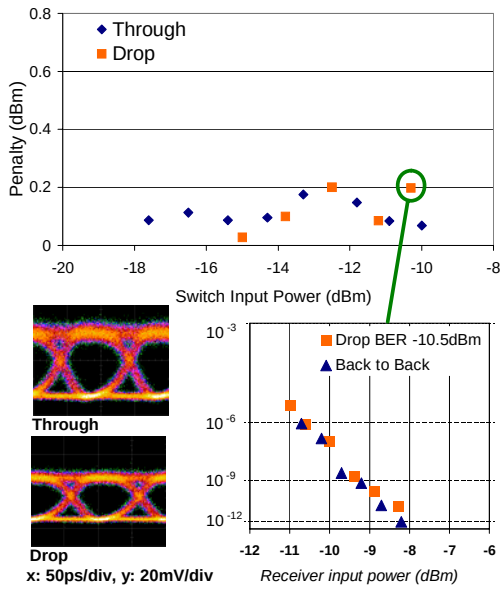

Fig. 5: Receiver power penalty as a function of switch input power along with representative BER curve and eye diagrams for the 'through' and 'drop' paths.

The results of the experiment are presented in Figure 5, showing the received power penalty as a function of input power into the 2x2 quantum SOA switch. These results show that this device has a potential of more than 8dB dynamic range for the through path and 5dB dynamic range for the drop path, for a power penalty of 0.2dB and below. The measurements are only performed for input powers from around -10dBm to -18dBm for the through path, and from -10dBm to -15dBm for the drop path, limited by the available power budget into the switch and receiver. The sensitivity of the receiver limits the measurements for lower input powers into the switch, whilst the input powers above -10dBm are limited by the output power of the tunable laser. The discrepancy between the minimum measurable input power of the through path and the drop path is due to the smaller on-chip gain attainable for the drop path. The gain difference between the through and drop path is around 2.8dB owing to the differences in splitting ratios of the TIR mirrors, as explained previously This accounts for the 3dB difference in dynamic range measurement for the two paths.

Discussion

High port-count switch architectures can be built up from cascades of 2x2 switches. For example, a 16x16 Benes network would comprise 56 2x2 switches arranged in 7 cascading stages. With a gain maximum of 12.1dB for the through path and 9.3dB for the drop path at a 100mA switching current, this 2x2 switch is able to provide enough power budget to overcome the losses from filters and isolators that may be required between switching stages. Large input power dynamic ranges relax the power margin for switch operation, giving the potential to support additional splitting stages prior to the switch fabric. This is important when additional intelligent control circuitry is built around the switch fabric. Examples of intelligent switch controls include the use of out-of band headers for switching time slots allocation [8], power equalization [9] and fault detection & restoration [10]. The low penalty operation suggests acceptable performance after cascades of the 2x2 switch [11][12].

Conclusion

This paper presents the design, fabrication, and system performance of a 2x2 quantum dot SOA based switch. Full, non-blocking 2x2 switching is achieved by biasing the appropriate QD SOAs in the switch. The maximum on-chip gain is 12.1dB, with power penalty of less than 0.2dB observed over an input power range of 8dB, and noise figure of 7.4dB. The high gain characteristics, low noise performance and extremely low penalty makes this novel integrated QD switch an ideal candidate for large scale high speed optical switching applications.

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