# Reactive Ion Etching in Silica-on-silicon Planar Waveguide Technology

Haiyan Ou

COM centre, Technique University of Denmark (DTU),
2800, Kgs. Lyngby, Denmark
ho@com.dtu.dk

Reactive ion etching has a wide range of applications in optical waveguide fabrication and is the enabling technology for hybrid integration. The etching mechanism, etch rate, mask material, and selectivity over mask are discussed for core etching, deep glass etching and deep silicon etching.

**Key words**: reactive ion etching, silica-on-silicon waveguide, groove

## Introduction

Since in 1969 Miller proposed the concept of integrated optical circuits (IOC)[1], it has evolved tremendously, especially during the past decade. Silicon was first used as the integration platform and it still has the prominent role until now, which can be ascribed to historical reasons. Long before the dawn of IOC, silicon-based microelectronics technology had been fully developed. Transferring the technology of silicon from microelectronics directly to photonics gives silicon-based IOC technology a substantial headstart. However, silicon is an indirect bandgap semiconductor, and it is very hard to realize efficient light emission and detection. Limited by this property, silicon was only confined to passive IOC, and indium phosphide (InP) was used as IOC platform for active and passive integration [2]. Compared to the silicon platform, InP is of direct bandgap, but it is expensive, and its high refractive index results in compatibility problems with standard fibres. Thus, both material platforms have advantages and drawbacks. Hybrid integration on a silicon platform takes advantage of both material platforms [3].

Different kinds of materials have been applied in silicon-based waveguide technology, such as germanium (Ge) doped glass [4], silicon oxynitride [5], and silicon nitride [6]. Reactive ion etching (RIE) is a key process to define the core geometry of the waveguides, and to etch deep structures across waveguides, which enables hybrid integration. In our cleanroom, Ge-doped glass waveguides on silicon substrate (silica-on-silicon) have been developed. In this paper, etching of glass and silicon using RIE is optimised with regards to the mechanism, mask material, selectivity over mask material, etch rate, sidewall roughness and sidewall angle.

## Waveguide fabrication

Waveguide fabrication consists of five main steps: buffer layer growth, core layer deposition, photolithography, core layer etching and top-cladding layer deposition, in which eight processing steps are utilized as: 1) Wet oxidization of the silicon wafer to form a thick silica buffer layer; 2) Deposition of Ge-doped silica to form the core layer by plasma enhanced chemical vapour deposition (PECVD); 3) Spinning and baking of photoresist on wafer; 4) Exposure of photoresist, transferring the waveguide structures from the photolithography mask to the photoresist; 5) Development of photoresist; 6) Etching of the core pattern using RIE; 7) Stripping of photoresist; 8) Deposition of boron and phosphorus co-doped silica to form the top cladding layer by PECVD, with refractive index matched to that of the buffer layer.

During the development of silica-on-silicon planar waveguides, fabrication processing is optimised step by step to achieve best performance and cost ratio. For hybrid integration the

performance is further complicated by the coupling between various elements as these are required to obtain different functionalities. For example, polarization independence of an IOC is becoming more and more important in applications within high bite rate telecommunication. One way to insure polarization independence is by inserting a half-wave plate in the middle of a symmetrical component [7]. Etching of deep grooves across a waveguide and into the silicon substrate therefore becomes a crucial process, requiring an optimised RIE process. A schematic view, demonstrating a groove cutting through the waveguide and into the silicon is shown in Fig. 1.

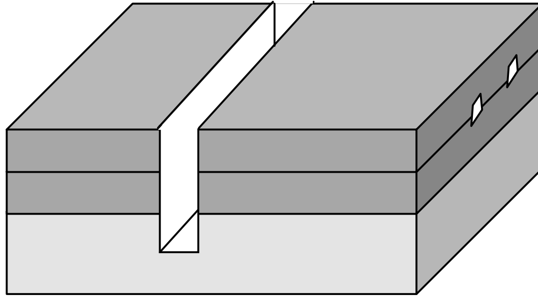


Fig. 1 A groove etched through the waveguide

In Summary, the application of RIE on silica-on-silicon planar waveguide consists of glass etching and silicon etching. Moreover, glass etching is used for two purposes: to define the geometrical structure of the core layer for the waveguide and to form deep grooves. The Silicon etching is performed to extend the groove deep into the substrate.

**Mechanism of glass and silicon etching**

The main parameters for the RIE process are the gas mixture, the applied RF power, and the chamber pressure. Other parameters such as the configuration of the etch chamber, the masking material on the wafer, and the design of the mask will also affect the etch process. In our cleanroom facilities a fluorine based gas mixture consisting of $CF_4$ and $CHF_3$ is used for the glass etching.

The etch process is dependent on the required functionality of the structure. Light is guided in the core layer, which requires that the sidewall and the top surface of the core are smooth, i.e. without roughness, particles and contamination. The core structures subsequently have to be covered by a PECVD glass layer. A slightly sloped sidewall is favourable with respect to step coverage. Photoresist was chosen as masking layer for this purpose because of the simplicity and the sloped and smooth sidewall. On the other hand, deep glass etching requires vertical sidewalls and a high etch rate. Poly-silicon is selected as the mask layer with regard to its high selectivity towards glass.

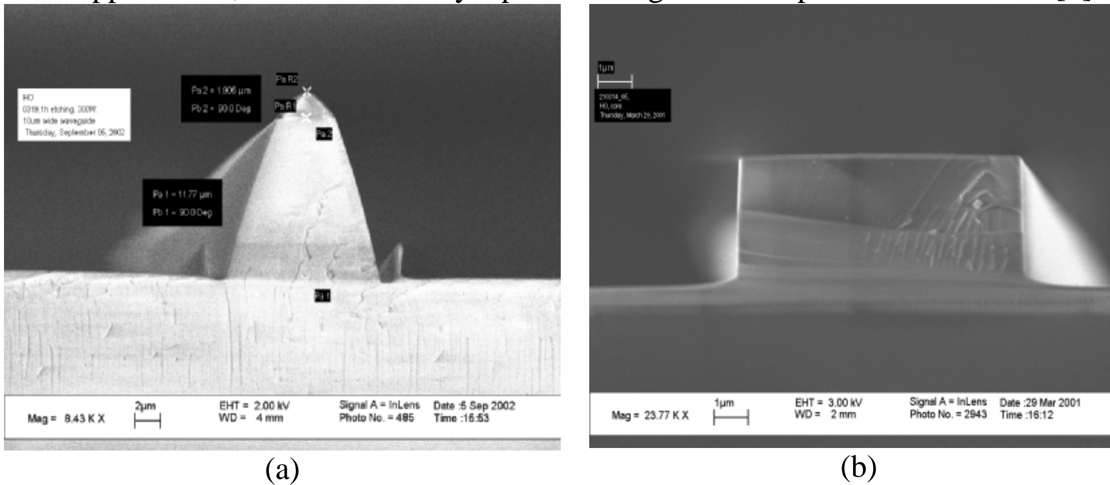
When deep etching of silicon into the substrate, the etched glass layer turns into the mask layer. Therefore, we use SF6 for silicon etching, which has a higher selectivity towards glass and exhibits a higher etch rate in silicon than the freon gasses.

**Results and discussion**

To arrive at optimised processing we need to categorize our results into three subsections, glass etching to define the geometrical structure of the core layer, deep glass etching to form a groove, etching into silicon to achieve a deep groove reaching into the substrate.

1) *Glass etching to define the geometrical structure of the core layer*

The etch process for the core layer, used to define the structure of the waveguide, has been fully optimised resulting in a record low propagation loss of 0.01 dB/cm. To our knowledge this is the lowest propagation loss ever reported. A big advantage of using photoresist as mask layer is that the sidewall angle of the core layer can be engineered by adjusting the thickness of the resist, as shown in Fig.2 (a) and (b). From the coupling point of view, a square core with vertical sidewall is desired to have a low coupling loss with standard fibres. However, a core layer with angled sidewall has other applications, such as vertically tapered waveguides for spot-size conversion [8].




(a) (b)

Fig. 2 Cross-section profile of angled (a) and vertical (b) glass etching by adjusting the thickness of the mask layer. Resist is still on top of the glass in (a). The etch rate is about 0.12 μm/min. and the selectivity over photoresist is about 5.

2) *Deep glass etching to form a groove*

Resist is excluded in the deep glass etching because fine structures are hard to obtain when thick resist is spun on to act as deep glass etch mask (limited by the aspect ratio of the photoresist). Poly-silicon was applied as the mask layer for the deep glass etching. Fig. 3 shows a SEM picture of a deep and vertical groove. The groove is about 15 μm deep, with smooth sidewall and flat bottom.

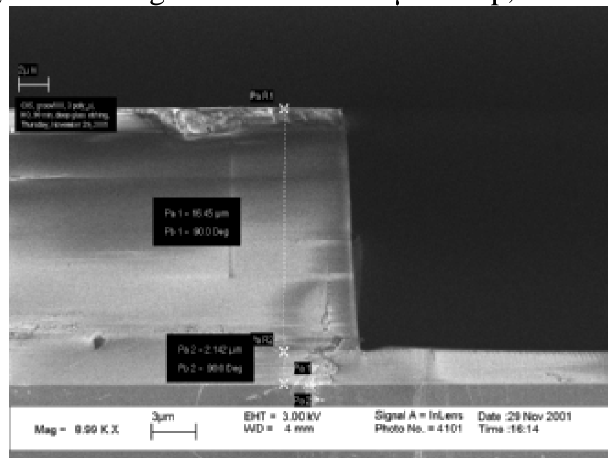



Fig. 3 Cross-section profile of a 15μm deep and vertical groove. The etch rate of glass is 0.24μm/min., and the selectivity of glass over poly-silicon is about 6. The mask layer is still on top of the glass.

3) *Silicon etch for the deep groove into the substrate*

When the groove was etched through the glass into the silicon substrate, glass becomes the mask layer. A SEM picture of a deep groove etched into the silicon substrate is shown in Fig. 4. The

etched thickness of the glass layer (cladding, core and buffer) is about 30 μm, and the etch is continued down into the silicon for another 80 μm. It can be seen that the silicon layer is under etched. By varying the oxygen concentration in the gas mixture, a passivation layer can be formed on the silicon sidewall. This will allow a vertical sidewall.

Fig. 4 Cross-section profile of deep silicon etching into the substrate. The etch rate of silicon is 1.12 μm/min, and the selectivity over glass is about 12.

**Conclusion**

The application of RIE in silica-on-silicon planar waveguide technology includes imprinting of a waveguide structure into the core layer and groove etching. Etching mechanism for core glass, thick glass and thick silicon in the formation of grooves is described. The core was etched with photoresist as mask, and record low propagation losses of 0.01 dB/cm have been obtained after optimisation. A poly-silicon mask was employed for the deep glass etch enabling a high etch rate and smooth vertical sidewalls. Deep silicon etching was shown to have a very high etch rate of 1.12 μm/min with the glass mask and optimisation with respect to the underetch is in progress.

**Reference**:

[1] S. E. Miller. *Bell Syst. Tech. Journal*, **48(7)**, 2059-2069, 1969.
[2] Smit, M.K. *Optical Fiber Communication Conference 2000,* **2**. 76, 2000.
[3] M. Kawachi, *Optical and Quantum Electron.*, **22**, 391-416,1990.
[4] S. Suzuki, M. Yanagisawa, Y. Hibino, and K. Oda, *J. Lightwave technol.* **12 (5)**, 790-796, 1994.
[5] M. Bohn, F. Horst, and B. J. Offrein, et al, *ECOC' 02,* paper **4.2.3**, 2002.
[6] W. E. Swendsen, H. T. Philipp, M. Svalgaard, et al, *ECOC' 02,* paper **4.2.4**, 2002.
[7] H. Takahashi, K. Oda, H. Toka and Y. Inoue, *J. Lightwave Technol.* **13**, 447-455, 1995.
[8] A. Sugita, A. Kaneko, and K. Okamoto, et al, *IEEE photonics Technol. Lett.,* **12**,1180-1182, 2000.