

# **A novel technique for high precision measurement of alignment accuracy of single-mode optoelectronic components**

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We describe technologies for cost-effective assembly of single-mode optoelectronic components, and report a novel technique to verify with sub-micrometer precision the alignment accuracy by flip-chip soldering.

**Keywords:** self-alignment, flip-chip, low-cost, assembly, single-mode, alignment accuracy, measurement method, moiré-effects

## **Introduction**

In the world-wide communication network the traffic is still increasing, in particular the internet traffic, and the access networks will soon become a bottle neck. An increasingly important part of the access network is the radio access network. For the next generation of high capacity mobile communication system distribution of signals into a dense mesh of radio base stations is crucial. The access networks thus need to be upgraded in the near future, and it is highly desirable to introduce optical single mode technology.

For transceivers developed for the trunk network, issues such as performance and long term reliability has been of prime interest and there has been no strong driving force to reduce the production cost. In this new scenario single mode optoelectronic components such as transceivers will be needed in very large volumes compared to the transport network and the cost for each component will not be shared by as many users as in the transport network. This will require that key optoelectronic components can be produced at substantially lower cost than previously.

## **Assembly of optoelectronic single mode components**

Some key technologies that can contribute to lower cost for optoelectronic devices are

- ◆ hybrid integration
- ◆ passive alignment
- ◆ non-hermetic encapsulation

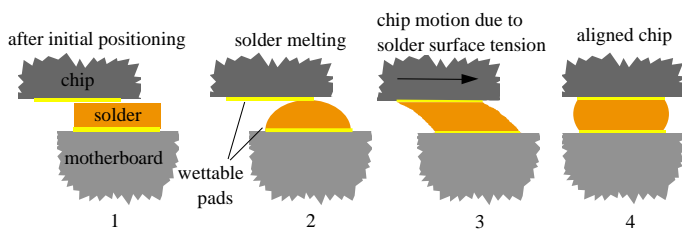
We will here in particular discuss passive alignment. Active alignment of, e.g., semiconductor lasers, requires that they are electrically connected. The alignment is iteratively optimised until coupling from the laser diode into a fiber is maximized. Using passive alignment electrical connections are not required. The electrooptical components are instead appropriately positioned using alignment marks or similar techniques. Several alternative methods for passive alignment have been reported, in particular:

1. Soldering using an infrared vision systems in combination with registration marks, so that alignment can be verified by IR radiation penetrating through carrier and semiconductor component [1,2]. The laser is positioned with high accuracy before it is soldered in place, and held in position during soldering
2. A soldering method similar to the previous technique, but based on very high precision mechanical system in combination with a computer controlled vision-system [3]. By observing the alignment marks before the parts are put into position, and relying on high precision mechanics, optical systems in the visible can be used.

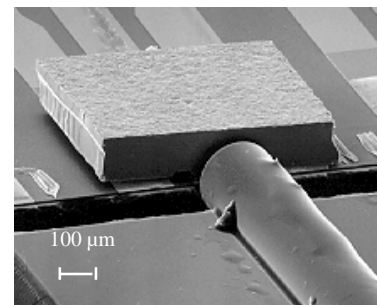
- Self-aligning flip-chip soldering. The laser diode is placed roughly at the correct position, e.g. using a pick and place machine. The surface tension of the solder bumps is utilized to achieve self-alignment of the laser diode to the proper position [4,5], possibly in combination with standoffs or stops [6,7].

Method 1 and 2 above are well suited for mounting one chip on each carrier, but more difficult to apply in other cases, in particular difficult to extend to wafer level assembly. The third method – on the other hand – can be used to mount several components on the same carrier and is compatible with batch soldering as well as wafer level assembly. Furthermore the moderate requirements on the initial positioning of the components makes the method compatible with conventional moderate performance pick-and-place-equipment.

We have developed a version of the self-aligning method [8,9]. The basic alignment principle is



**Figure 1** Schematic illustration of the self-alignment principle



**Figure 2** SEM picture of a flip-chipped diode laser self-aligned with respect to an optical fiber

schematically shown in Fig. 1. An example of a flipchip soldered laser diode is illustrated in Fig. 2 [8]. We have used this self-aligning-soldering technique to mount individual laser-diodes as well as array lasers versus fiber-grooves or polymer waveguides. Within the framework of a technology demonstrator for an array transceiver module we have furthermore mounted both an array laser and an array detector on each carrier [10]. The two components are positioned epi-side down on the appropriate solder pads on the carrier, and then both soldered in place in the same sequence and self-aligned to their proper positions

### High precision measurement of alignment accuracy

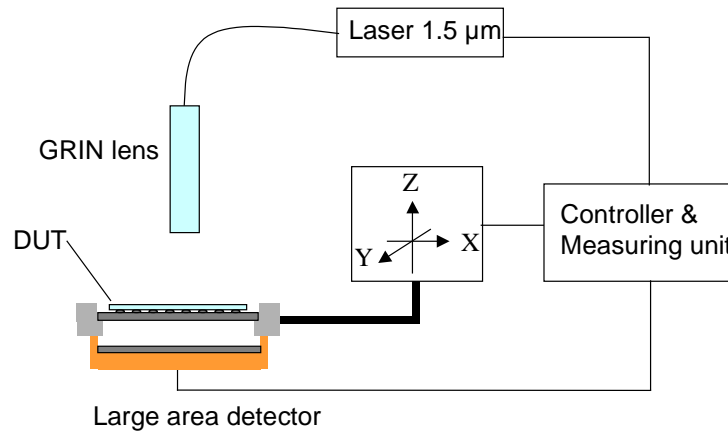
When using passive alignment it would be of great interest to be able to measure with sub-micrometer accuracy the position of the chip versus the carrier. From a yield point of view, it is important to obtain this information as early as possible, before the following assembly steps. Such measurements are, however, difficult:

- The semiconductor chip is typically not diced or cleaved with enough accuracy so that the outer edges of the chip can be used as reference points for a measurement.
- Alignment marks need to be on the top face of the carrier and on the downside epi-face of the semiconductor chip. They are thus hidden between non-transparent substrates and difficult to evaluate with high accuracy.

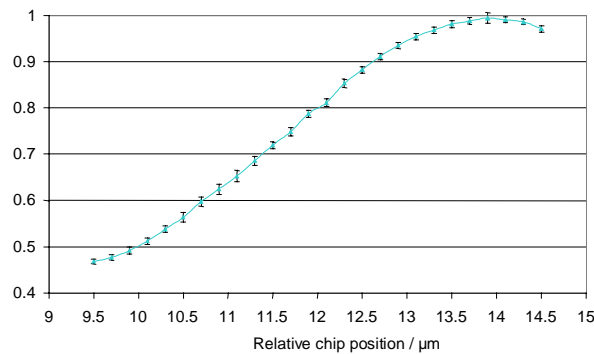
We have developed a method based on moiré-effects, which requires only an infrared laser diode and a single photodetector together with standard electronics for evaluation. No infrared imaging optics is thus needed which strongly simplifies the implementation of the method. A periodic pattern – with a typical feature size of about five micrometers, well within standard processing limits – is formed in a metal layer on the carrier. This together with a similar pattern on the chip to

be mounted form a moiré-like pattern which can be analysed in real time during solder reflow, or, more conveniently, in a measurement phase after the soldering cycle. Various types of moiré and Vernier patterns are used to facilitate and evaluate alignment, for example with mask-aligners. Our evaluation technique, however, is novel to the best of our knowledge.

Silicon carriers and dummy chips have been fabricated. Electro-plating was used to form the solder-bumps of Au-Sn. Our first experimental tests of the method were carried out by moving a chip versus a carrier. The experimental evaluation set up is illustrated in Fig 3 and typical experimental results are shown in Fig 4. As seen in the figure a sub-micrometer resolution can be achieved.

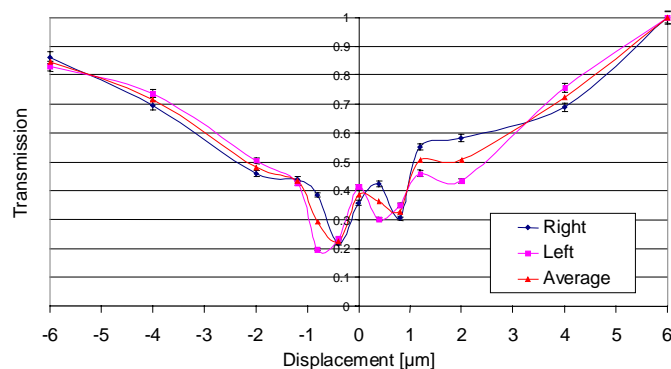


**Figure 3** The set-up for verification of alignment accuracy. A fiber coupled 1.5 μm laser illuminates the moiré-pattern and a large area detector detects the transmitted light.



**Figure 4** Output signal versus relative position for chip with respect to carrier.

In the next step we have started to do measurements after that chips have been soldered in place on carriers. In this case a somewhat more complicated pattern was used. Promising results have been obtained, illustrated in Fig 5. A number of measurements were done at different positions on the same chip. The method is designed in such a way that the minimum signal is obtained for the actual chip displacement, in this case about 0.4 μm. Further measurements are underway and analysis and more details will be reported at the conference.



**Figure 5** Measurement of alignment accuracy for chip self-aligned on silicon carrier, in this case indicating a displacement of about 0.4  $\mu\text{m}$

**In conclusion:** Self-aligning flip-chip soldering is a promising method for cost-effective assembly of single-mode optoelectronic modules. The method would be even more valuable if the position accuracy could be easily monitored or verified. We have developed a measurement technique, which combine sub-micrometer resolution with a comparatively simple and inexpensive evaluation equipment. The method could be used during solder reflow to monitor the process or after soldering to verify the results, as well as in future wafer level assembly.

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